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Proximity focusing RICH with aerogel as radiator

Doctoral Thesis

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Detektor obročev Čerenkova s sevalcem iz aerogela

Disertacija

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Zahvaljujem se mentorju prof. dr. Samu Korparju, somentorju dr. Roku Pestotniku ter vodji raziskovalne skupine prof. dr. Petru Križanu. Hvaležen sem za napotke, nasvete, pomoč, potrpljenje in nepozabne trenutke. Eriku Marganu in Juretu Eerženu se zahvaljujem za tehnično podporo, ter podjetju Cosylab d.d. za pomoč pri izvedbi doktorata. Nenazadnje zahvalo za potrpljenje in podporo si zaslužijo tudi punca Maja ter starši in sorodniki.

Abstract

The Aerogel Ring Imaging Cherenkov (ARICH) detector will be installed in the Belle II spectrometer at KEK institute in Tsukuba, Japan. The detector is comprised of an aerogel radiator, an expansion volume, and a detector plane composed of position sensitive single photon detectors. The photon detectors need an electronic readout system which will have to operate in the Belle II experimental environment. The thesis describe the design, construction and tests of an electronic system which fulfills the requirements. The electronic readout board was tested for operation in the magnetic field and in presence of ionizing radiation. Finally, a test with charged particle beams confirmed the performance of the ARICH detector with the readout system as discuussed in this thesis.

Keywords: Cherenkov radiation, PID devices, photon detection, electronics and devices, ASICs, FPGA, sensors, radiation tolerance

Povzetek

Detektor obročev Čerenkova z aerogelom kot sevalcem bo vgrajen v spektrometer Belle II ob elektronsko-pozironskem trkalniku v institutu KEK v Cukubi na japonskem. Detektor sestavljajo sevalec iz arogela, ekspanzijski prostor in detektorska ravnina. Detektorska ravnina je sestavljena iz pozicijsko občutljivih senzorjev posameznih fotonov in čitalne elektronike. Slednja mora biti sposobna delovati v zahtevnem okolju eksperimenta, v magnetnem polju 1.5 T in v polju ionizirajočih sevanj in nevtronov. Doktorsko delo obravnava konstrukcijo, izvedbo in preizkus takega čitalnega sistema. Povzema tudi preizkus detektorja obročev Čerenkova v curku nabitih delcev.

Ključne besede: Sevanje obročev čerenkova, naprave za identifikacijo delcev, detektorji za fotone, elektronska vezja, ASICs FPGA, senzorji, sevalne poškodbe

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1 Introduction

Experiments in High Energy Physics (HEP) often use particle accelerators for studies of elementary particles and their interactions. In a typical HEP experiment accelerated particles are either collided against a fixed target or against a beam of particles circulating in the opposite direction.

The point where particles collide is called the interaction point. A spectrometer built around the interaction point measures decay products of particles that are created during the collision. The spectrometer is composed of a number of sub-detectors. These detectors measure momentum, energy and speed of the produced particles. Data collected from all detectors are sent to an acquisition system which stores them until for further analysis.

One of the most important features of the spectrometer is to identify the interaction products. The identification of charged particles with momenta in the kinematic range from 1 GeV/c to 100 GeV/c can be efficiently carried out with the use of Ring imaging Cherenkov (RICH) detectors. This kind of detectors are used to measure the speed of charged particles. Combing this measurement with the data from other detectors which provide the value of the momentum of the particle, the mass of the particle can be determined, and the particle can thus be identified.

At the KEK institute in Tsukuba, Japan, an international research group is upgrading its previous experiment called Belle. The upgraded experiment (Belle II) aims to collect a 50 times larger data sample. In the new spectrometer, a RICH detector with aerogel radiator (known also as ARICH) will be used to indetify particles in the forward region.

The present thesis is structured as follows. In the introductory chapters I will briefly describe the Belle II spectrometer, review Cherenkov detectors and discuss the ARICH detector. I will then proceed with the main topic, the readout system of ARICH. The readout system is composed of electronic readout boards which record, process and store events during the detector operation. I will present various aspects and limitations which have to be considered during the design process of the readout electronics for this specific case. My work covers the design and construction of electronics boards, including the selection of components, schematical designs of the system components, and the readout board production. A further chapter is dedicated to the programming of the system. The following chapters describe tests of the readout system in laboratory conditions, as well as tests in harsh environments. Finally, a test in a beam of charged particles is discussed which was used to verify the overall performance of the detector.

2 Belle II experiment

The basic objective of the international group of physicists in the Belle II collaboration is to study rare decays of B and D mesons and τ leptons. In collisions of electrons and positrons, B meson pairs are created. B mesons are short lived particles that decay through various decay chains into stable charged and neutral particles, pions, kaons, protons, neutrons, muons, electrons, gamma rays and neutrinos. The Belle experiment at the KEK Institute in Tsukuba, Japan, collected more than 700 million $B\bar{B}$ pairs during 10 years of operation [1]. With accurate measurements of B^0 and $\bar{B}^0$ meson decays, the Belle group succeeded in measuring slight differences in both decays. Measurements of CP violation in the B meson system, that were made by Belle and BaBar (a similar international research group at Stanford, USA [2]), confirmed the predictions of theoretical physicists M. Kobayashi and T. Maskawa [3]. With the new spectrometer Belle II at the same collider, the research group aims to collect a 50 times larger data sample of $B\bar{B}$ pairs. For this purpose, the KEKB collider and Belle spectrometer will be upgraded. The new collider, SuperKEKB, will have a significantly increased luminosity. This implies a redesign of the Belle detector in order to cope with a higher event rate and increased background levels. The new Belle II detector will be built inside the support structure of the old Belle spectrometer.

2.1 KEKB collider

KEK-B was the particle accelerator used in the Belle experiment [4]. It is an asymmetric positron (3.5 GeV) and electron (8.0 GeV) collider having 3 km of circumference, installed 11 meters below the ground level.

The beam energies are chosen so that the center of mass (CM) energy is E_{CM}=10.58 GeV which corresponds to the mass of the Υ(4S) resonance. This is just above the threshold for the B meson production, and as it turns out,Υ(4S) decays exclusively to a pair of B mesons. Because at such a collider a large number of B mesons can be produced, KEKB is called a B-factory.

The complex accelerator system is composed of a source of electrons and positrons, a linear particle accelerator and two storage rings. Electrons are usually generated by a cold cathode, a hot cathode, a photocathode, or radio frequency (RF) ion sources. Positrons are created by hitting a tungsten target with relativistic electrons where a part of the energy released in collisions is used to create electron-positron pairs. A magnet captures the emerging particles, and redirects the positrons into the linear accelerator where they are accelerated in a similar fashion as electrons. The linear accelerator greatly increases the energy of charged particles by subjecting them to a series of oscillating electromagnetic fields. Charged particles are grouped

into bunches. The narrow beam of accelerated bunches is then directed into the storage rings of the KEK-B collider. The two rings have four straight sections. Within the straight sections RF cavities supply energy to the particles to compensate for the energy lost due to synchrotron radiation. A schematic view of the KEK complex accelerator system is in Fig. 1.

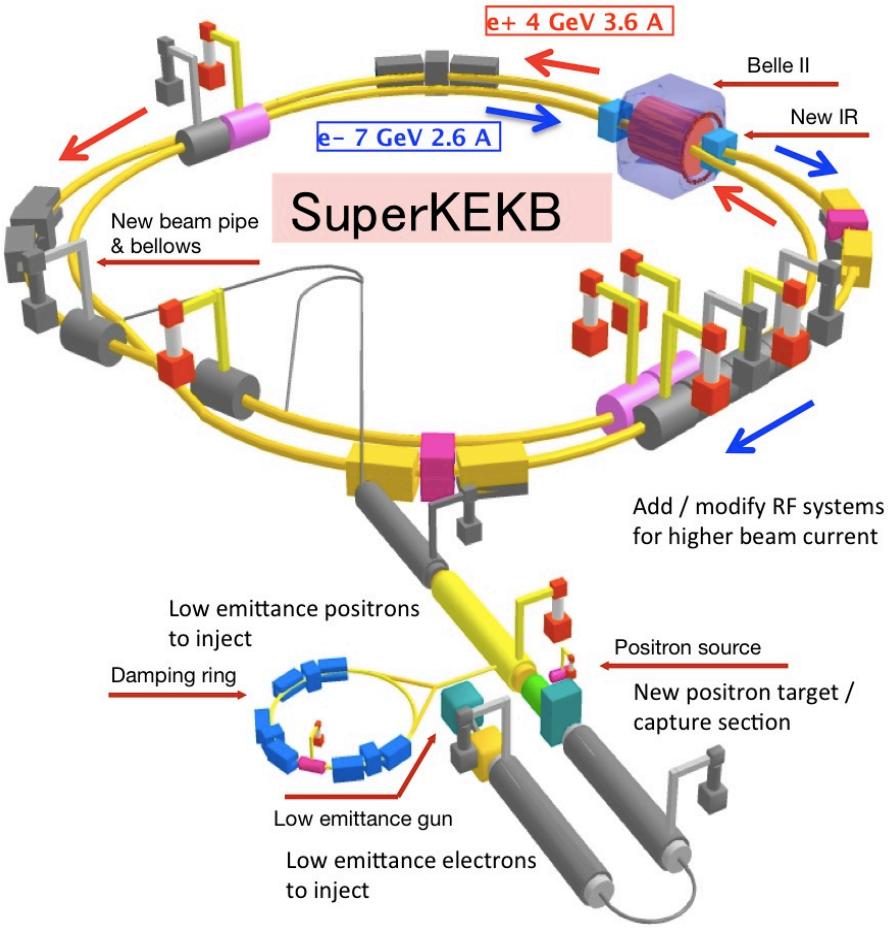


Figure 1: SuperKEKB accelerator facility.

The main parameter of a collider is the luminosity L, the proportionality factor between the reaction rate dN/dt and the cross section σ for the reaction, $dN/dt = L\sigma$. The luminosity can be expressed in the following way:

$$L = \frac{Ne^- Ne^+ f R_L}{4\pi\sigma_x^*\sigma_y^*}, \tag{1}$$

where e^+ and e^- denote positron and electron bunches, N is the number of particles per bunch, f is the collision frequency, σ_x and σ_y are the horizontal

and vertical beam sizes at the interaction point, and R_L is the luminosity reduction factor. KEK-B has one interaction point, where the electron and positron beams collide at a finite angle of 11 mrad.

KEKB was the world's highest luminosity machine. A record luminosity of $2.11 \times 10^{34}\ cm^{-2}s^{-1}$ was achieved in June 2009. For the Belle II experiment the accelerator will be upgraded. In the new SuperKEKB collider the luminosity will be increased by dramatically shrinking the beam size and modestly increasing the beam currents, as well as by optimizing the beam optics in the interaction region.

2.2 Belle II spectrometer

The new Belle II spectrometer is a hermetic detector of elementary particles constructed around the interaction point. The redesigned detector needs will have to cope with a 20 times increased level of the beam-induced background compared to the previous experiment. The background sources include scattering of the beam on residual gas in the beam pipe, Touschek scattering, synchrotron radiation, and some of the high rate electron positron interactions at the interaction point, like Bhabha and radiative Bhabha scattering, $e^-e^+ \to e^-e^+$ and $e^-e^+ \to e^-e^+\gamma$ [5]. Another important aspect is the event rate which will be about 10 times higher. This implies a faster trigger logic and a more powerful data acquisition system.

The Belle II spectrometer (Fig. 2) is comprised of the following subsystems:

- *Iron yoke* which acts as a return yoke of the magnet as well as support structure and absorber of the muon detector;
- *Superconductive magnet with* a 1.5 T magnetic field;
- *Vertex Detector* - VXD;
  The silicon vertex detector measures B and D meson decay vertices. It is the innermost detector placed around the beam pipe. It consists of four layers of double-sided strip detectors and two layers of pixel detectors.

  Central Drift Chamber - CDC;
  is used to reconstruct charged particle tracks with good precision from which momentum can be determined with sufficient resolution. It also provides particle identification based on the characteristic energy loss (dE/dx) for pions, kaons, protons at up to about 1 GeV/c momentum.
- *Electromagnetic calorimeter* - ECL;
  The ECL is built of CsI crystals and measures the direction and the energy of high energy gamma rays.

- *Time of propagation* - TOP;
  TOP is a particle identification device. It identifies a charged particle by means of detecting internally reflected Cherenkov photons inside a quartz radiator. At one end of the quartz radiator, an array of position sensitive photon detectors measures the position and time of arrival of the Cherenkov photons from which the velocity can be extracted. The quartz bars are positioned on a cylindrical surface around the CDC.

- *Aerogel RICH* - ARICH;
  It is a particle identification device which measures the particle velocity using Cherenkov rings. It is designed to provide efficient separation of pions and kaons from 1 GeV/c to 4 GeV/c in the forward end-cap of the spectrometer.

- *Neutral kaon K_L and muon detector* - KLM;
  It is built of multiple layers of charge particle detectors interspersed by iron plates in the iron return yoke of the magnet.

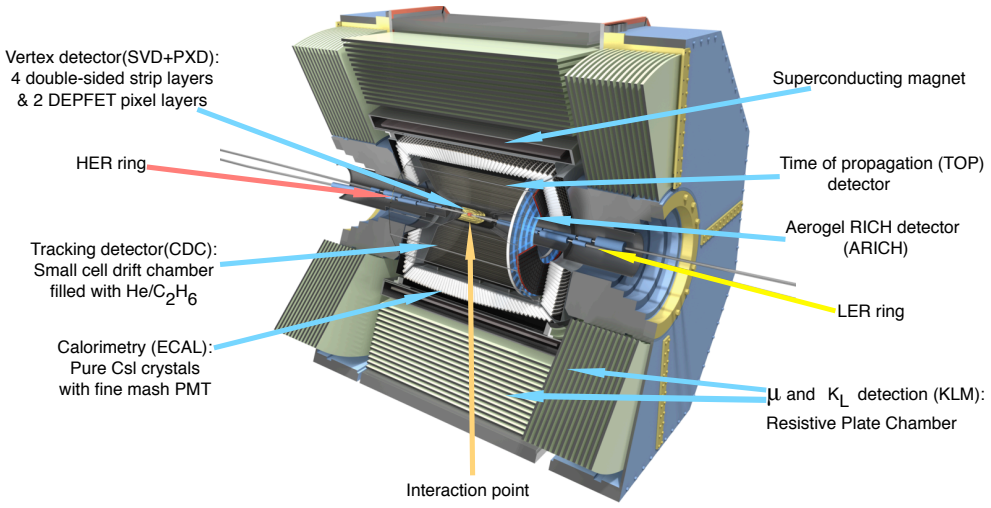


Figure 2: Cross section view of the Belle II spectrometer with its detectors.

3 Ring Imaging Cherenkov Detector with Aerogel Radiator

Ring Imaging Cherenkov detectors are one of the most important tools to identify particles in particle physics. In the forward region of the Belle II spectrometer, a proximity focusing RICH detector will be used. In this chapter, we will first discuss some basic properties of Cherenkov radiation and Cherenkov detectors, present the design criteria for the particle identification device in the forward region of the Belle II spectrometer, and present the final version of the elements of the counter.

3.1 Cherenkov radiation

Cherenkov electromagnetic radiation is emitted when a charged particle passes through a dielectric medium with a velocity v, greater than the phase velocity of light in that medium,

$$v > c_0/n \ , \tag{2}$$

where n is the refractive index of the medium, and c_0 is the speed of light in vacuum. The effect is named after the Russian scientist Pavel Alekseyevich Cherenkov who first observed and categorized it, and was awarded the Nobel prize in 1958.

The emission of light is induced by locally polarizing the medium while the charged particle passes through the dielectric. The dipole oscillations result in the emission of electromagnetic radiation. In case of a particle velocity lower than c_0/n, dipoles contributions interfere destructively, and no photons are emitted. In case the particle velocity is greater than c_0/n, an electromagnetic shockwave is produced as a consequence of the dipoles trailing the particle [6]. In Fig. 3, the electromagnetic shock wave travels over a distance $c_0 t/n$, while in the same time interval the particle moves by $vt = \beta c_0 t$, where $\beta = v/c_0$. The Cherenkov photon emission angle relative to the particle direction (θ) is given by:

$$cos\theta = \frac{1}{n\beta} \ , \tag{3}$$

The maximum Cherenkov angle for particles with $\beta = 1$ is therefore:

$$cos\vartheta_M = 1/n \ . \tag{4}$$

The number of emitted Cherenkov photons per photon energy interval and unit path length is [7]:

$$\frac{d^2N}{dEdl} = \left(\frac{z^2\alpha}{\hbar c_0}\right)\left[1 - \left(\frac{1}{n(E)\beta}\right)^2\right] \ , \tag{5}$$

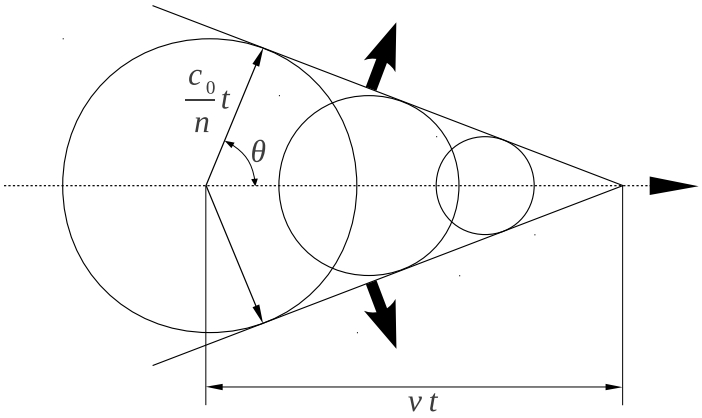


Figure 3: An electromagnetic shockwave, resulting from Cherenkov radiation.

where $\alpha = \frac{e_0^2}{4\pi\varepsilon_0\hbar c_0} \approx \frac{1}{137}$ is the fine structure constant.

3.2 Cherenkov detectors

Cherenkov radiation is often used in high energy physics for particle identification. A charged particle is identified if we know its mass. Cherenkov detectors are usually used in combination with tracking detectors that provide the information on the momentum of the particle. Combining the momentum and velocity as measured by a Cherenkov detector (Eq. 25) the mass can be obtained through the relation $p = \beta\gamma mc$.

The basic version of a Cherenkov detector includes a transparent radiator body with a suitable refractive index, an optical system (expansion volume or mirrors) and a photon sensor. Threshold Cherenkov counters use the property that Cherenkov radiation is emitted above a certain velocity of the charged particle (Eq. 6).

$$p_{threshold} = \frac{mc}{\sqrt{n^2 - 1}} \ . \tag{6}$$

This allows setting up a device with 3 identification intervals for particle momentum: an interval where the charged particle momentum is too low to be detected, an interval where lighter particles emit Cherenkov light before the heavier, and an interval where both species emit Cherenkov light. The threshold counters operate in the intermediate interval. Various implementations of these counters were used in spectrometers where a large solid angle needs to be covered, one example being the Belle Aerogel Cherenkov Counter (ACC).

In contrast to threshold Cherenkov counters, a Ring Imaging Cherenkov (RICH) detector measures the angle of the emitted Cherenkov photons. The

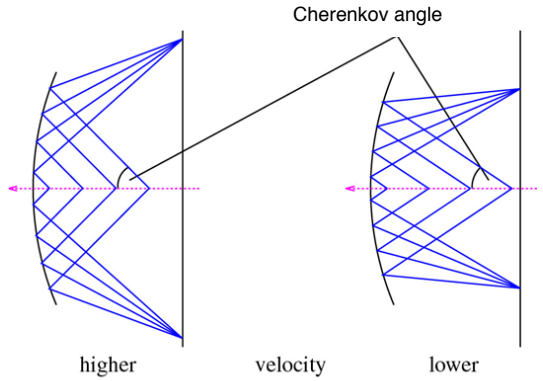


Figure 4: RICH detector with gas radiator.

principle of operation can be seen in Fig. 4. If a gas is used as a Cherenkov radiator, the path length of the particle needs to be of the order of few meters in order to acquire an adequate number of detected photons. A spherical mirror is used as an optical system, which focuses the photons onto the detector plane. The Cherenkov angle for different particle species in a typical RICH detector is shown in Fig. 5. In Fig. 6 we show the Cherenkov angle dependence on momentum for three different radiators, two gases and a solid radiator.

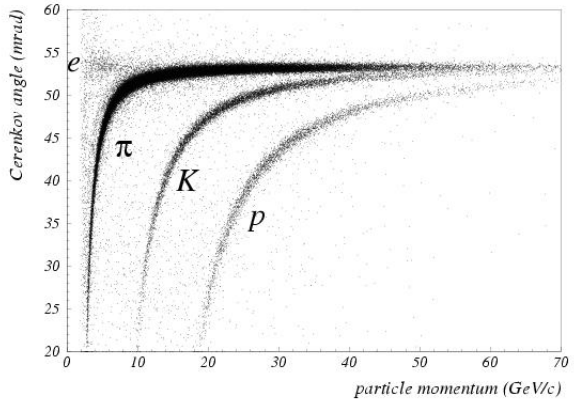


Figure 5: Measured Cherenkov angles for pions, kaons and protons for the HERA-B RICH with a gas radiator with $n \approx 1.0013$ and a single photon angular resolution of about 0.6 mrad.

An alternative to gas mixtures is the use of a solid radiator with a higher refractive index, where the radiator thickness of a few cm already results in a sufficient number of detected photons. In this case a gap is needed between the radiator and the detector plane (Fig. 110), but no mirror is required. This configuration is known as a proximity focusing RICH.

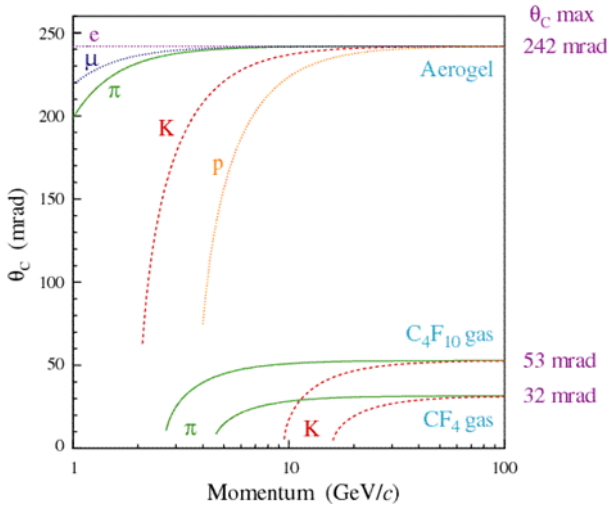


Figure 6: Cherenkov angle as a function of momentum for various radiators, two gases and a solid radiator.

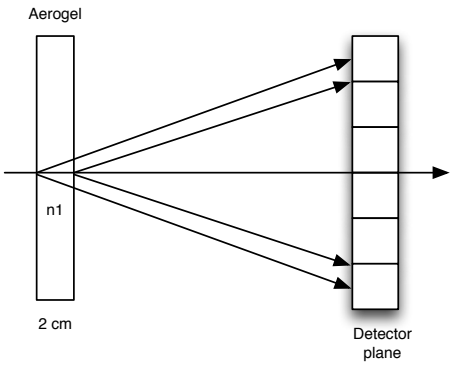


Figure 7: A proximity focusing RICH.

The uncertainty in the measurement of the Cherenkov angle depends on:

- Granularity of the photon detector
- Optical system quality
- Uncertainty in particle track parameters
- Multiple scattering of the particle in the radiator volume

The range of operation for RICH detectors is limited at low momenta by the minimal threshold velocity of the particle, and at high momenta by the measurement resolution of the Cherenkov angle. RICH detectors with solid radiators usually cover the momentum range from 1 GeV/c to a few GeV/c. Using gas mixtures with a lower value of n increases the operational range and can exceed 100 GeV/c (Fig. 6).

Another important fact determining the performance of the RICH counter is the number of detected photons. It is given by

$$N_{det} = L \int T_s(E) \cdot \epsilon(E) \cdot T_e \cdot \frac{d^2 N_c}{dE dL(E)} dE \ , \tag{7}$$

where L is the radiator length, $T_s(E)$ is the transmission of the radiator, $\epsilon(E)$ is a product of quantum efficiency and collection efficiencies, T_e is the efficiency of the readout system and $\frac{d^2 N_c}{dE dL(E)}$ is the number of emitted photons per per energy interval and particle path length trough the radiator, as given by Eq. 5.

Cherenkov detectors use a radiating medium made of transparent material with a refractive index which best suits the regime of operation (Figs. 6, 9). For gases, a typical refractive index value is about 1.001, for solids materials it is about 1.5.

Between these two options a very interesting material is silica aerogel, a light insulator with a refractive index ranging from 1.01 to 1.1. Silica aerogel is a highly porous solid structure of silica particles [8]; two examples are shown in Figs. 8 , 9. The transparent material contains a fine structure

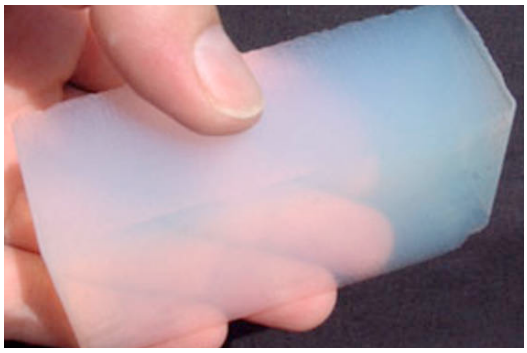


Figure 8: Aerogel material.

Figure 9: Aerogel tile [9].

silica network and air gaps with a size of about 10 nm. One of the problems in using aerogel as Cherenkov radiator is the removal of light due to Rayleigh scattering as can be seen in Fig. 8. The transmission of a sample of thickness d:

$$T = T_0 exp(-d/\Lambda(\lambda)) \ , \tag{8}$$

is a strong function of the wavelength, and turns out to depend on the refractive index and production method. Typical absorption length Λ for very good samples is about 40 mm at 400 nm.

3.3 Proximity focusing RICH with aerogel radiator for Belle II

In the forward region of the Belle II spectrometer (Fig. 10) a proximity focusing RICH with aerogel radiator aims to separate kaons from pions in the interval between 1 GeV/c and 4 GeV/c [9]. This fixes the refractive index between 1.04 and 1.06, and as a result, aerogel is the material of choice for this counter.

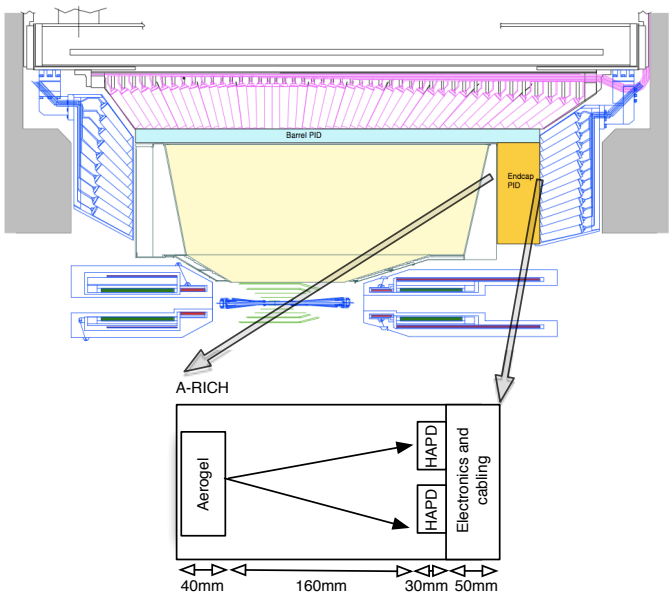


Figure 10: Belle II spectrometer with the ARICH detector.

The RICH detector with aerogel radiator (ARICH) is comprised of (Fig. 110):

- radiator
- expansion volume
- array of position sensitive photon detectors
- readout system for the photon detector

The available distance for the expansion volume in the upgraded Belle detector is approximately 20 cm. This limitation comes form the fact that the new system will be integrated into the volume of the old Belle aerogel threshold Cherenkov counter, and takes into account the thickness of the radiator (few cm) and of the photo-sensor with the read-out electronics.

The key parameter defining the performance of the detector is the Cherenkov angle resolution per charged particle for N detected photons,

$$\sigma_{track} = \sigma_\theta / \sqrt{N} \ . \tag{9}$$

In order to reliably measure the Cherenkov angle, at least 10 photons need to be detected by the photon sensor, and this can be achieved with a thick radiator. With a thick radiator, however, the single photon resolution would degrade because of the emission point uncertainty.

A solution to overcome this limitation is a proximity focusing RICH using a non homogeneous aerogel radiator shown in Fig. 11. Two consecutive aerogel layers with different refractive indices allow an overlapping of the Cherenkov rings on the detector plane, thus increasing the number of photons per ring without degrading the resolution[9, 10]. The data recorded with early

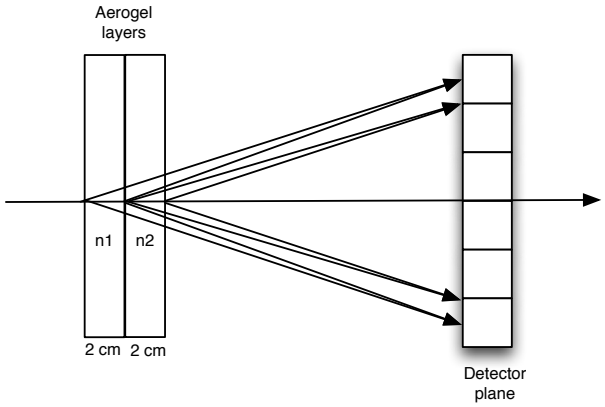


Figure 11: Focusing RICH with a double aerogel layer

prototypes reveal a clear improvement by the use of this focusing radiator configuration [9, 11]. Fig. 12 shows a comparison of the measured Cherenkov angle distribution for single photons with the use of a single aerogel having a refractive index of 1.046 (right) and two aerogels in the focusing configuration (n_1= 1.046, n_2 = 1.056 (left)). The single photon resolution for the focusing configuration is considerably better σ_θ=14.3 mrad compared to a single layer value, σ_θ= 20.7 mrad.

A number of sources contribute to the measurement error [9]. The total sum of errors from the aerogel thickness, distance to the photon sensor, photon sensor spatial resolution (4.9 mm $\times$ 4.9 mm pad size), chromatic error, variation of the refractive index over the energy range of Cherenkov photons that are detected by the photon detector, and aerogel inhomogeneity add up to σ_θ= 14 mrad for a single photon.

Finally we note that the proximity focusing ARICH for Belle II will use much of the available space for the expansion volume (Fig. 10). The space available for the readout electronics thus remains very limited.

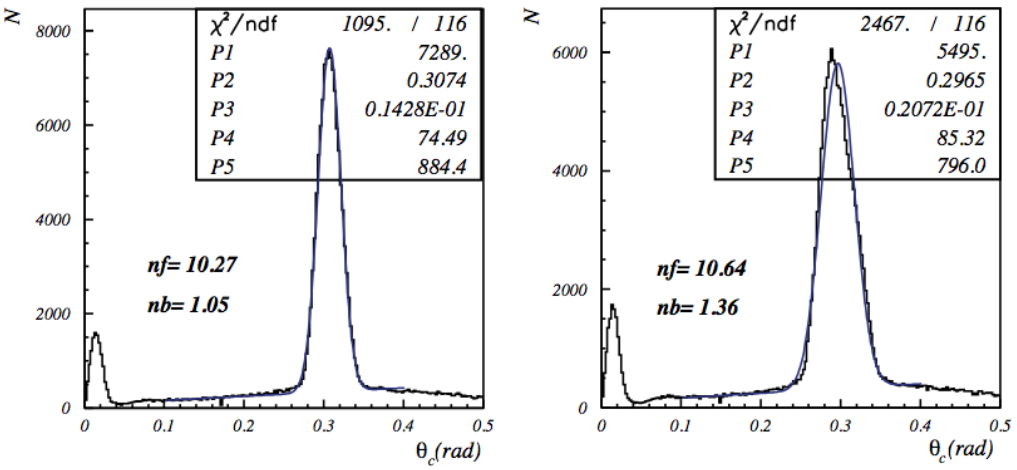


Figure 12: Comparison between proximity focusing RICH with an inhomogeneous aerogel (n_1= 1.046, n_2 = 1.056) 2 × 2 cm, and a single layer with a 4 cm thick layer [9].

3.4 Photon detector for ARICH

The most critical element of the ARICH detector is the position sensitive photon detector. It has to cover a surface of roughly 3.5 m^2(Fig. 13), has to be able to detect single photons with sufficient efficiency and spatial resolution, and has to be able to operate in a magnetic field of 1.5 T.

Photon detectors are used in many areas of physics research [12]. Useful applications of low level light sensors can be found in particle physics, astrophysics as well as medical devices such as positron emission tomography. In fact, quite some detectors in the high-energy physics, nuclear physics, and astrophysics rely on the detection of photons in or near the visible range 100 nm $\leqslant \lambda \leqslant$ 1000 nm. Differing in the type of operation and construction, photon sensors can nowadays cover quite well the entire visible wavelength spectrum. These sensors can be found in gamma ray detectors, Cherenkov detectors, calorimeters, etc. Depending on the type of operation, they are usually coupled to a scintillator, or other form of radiator, such as aerogel or a quartz bar. Best known single photon detectors are Photo Multiplier Tubes (PMT), Silicon Photo Multiplier (SiPM, also known as Multi Pixel Photon Counter - MPPC or Solid State Photomultiplier - SSMP) and Multi Channel Plate Photomultipliers (MCP PMT). Photon detection involves generating an electrical signal proportional to the number of incident photons. The detection usually involves generation of a primary photo-electron or an electron-hole pair by an incident photon. An amplification of the photo-electron signal brings the initial charge to a level suitable for detection. The last step is to collect the charge.

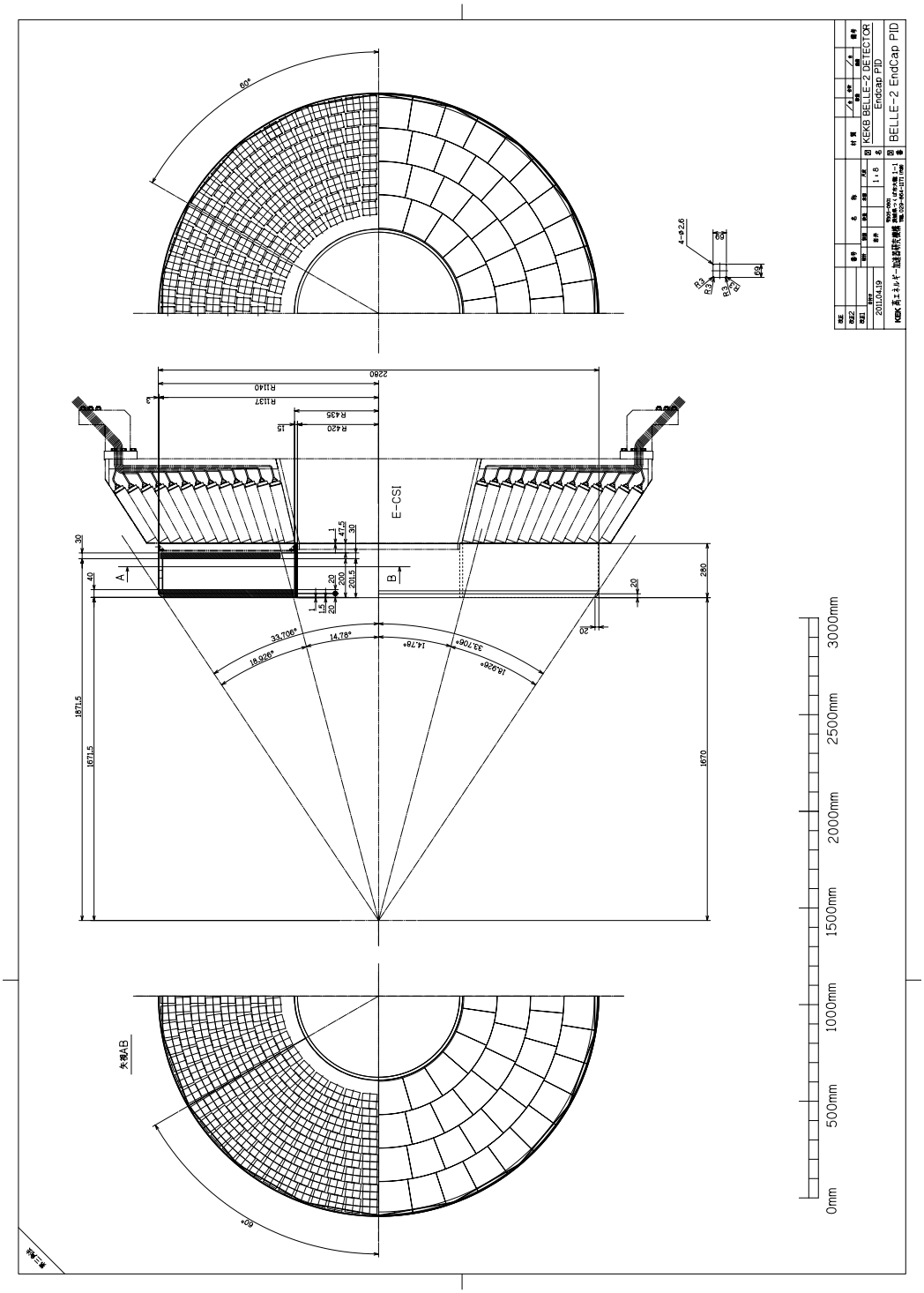


Figure 13: ARICH detector drawing / geometry of the detector / aerogel tiles and photon sensors.

The most important parameters of a photon sensor are [12]:

- Quantum efficiency (QE) - the average number of electrons generated per incident photon. ($0 \leqslant \mathrm{QE} \leqslant 100\ \%$)
- Collection efficiency (CE) - the acceptance factor other than the generation of photoelectrons. ($0 \leqslant \mathrm{CE} \leqslant 100\%$)
- Gain (G) - the number of electrons collected per incident photon.
- Dark count rate - the emission of electric signals, when no photons are present.
- Energy resolution.
- Dynamic range, the range of the maximal and minimal signal available from the device.
- Time dependence of the response including transit time, the time between the arrival of the photon and the signal formation. This affects timing resolution.
- Rate capability, time between two detected signals without pile up.

Each photon sensor concept has a potential to better serve a particular use. MCP-PMTs have excellent timing properties, single photon resolution and can operate in magnetic field but their drawback are aging effects which limit the lifespan of this devices. SiPMs are an interesting choice but suffer from radiation vulnerability while PMTs cannot be operated in high magnetic fields. The development in the area of photon sensors brought also a hybrid device called hybrid avalanche photo diode (HAPD) which is the sensor of choice for the ARICH detector [9].

The Hybrid Avalanche Photon Detector (Figs. 16 and 15), has been developed in a collaboration with Hamamatsu Photonics. The sensor combines the sensitivity of a PMT with the excellent spatial and energy resolution of a silicon sensor. In a ceramic enclosure, four APD chips are mounted each having 36 channels. The pad size is 4.9 mm $\times$ 4.9 mm (Fig. 14). The outer dimensions of the device are 72 mm $\times$ 72 mm $\times$ 30 mm. A quartz entrance window (Fig. 15) placed on the top of the device is coated with a layer of 20 nm bialkali photo-chatode on the inside. The distance between the photo-cathode and the APD chips is about 25 mm. Photons entering the bi-alkali photo-cathode on the inner side of a quartz window generate photo electrons which are accelerated along the electric field. The typical high voltage applied is between 7 and 10 kV. Accelerated photo electrons penetrate into the APD pixels (Figs. 14, 17). Their elevated energy is used to generate electron-hole pairs in the silicon. The high electric field inside

the APD produces avalanches adding an additional gain of 40 when the bias voltage is applied. The total gain is about 10^5. The device shows also an impressive ability of single photon detection (Fig. 18).

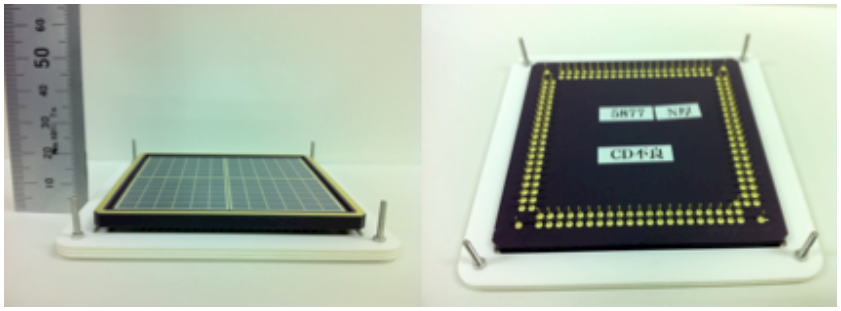


Figure 14: APD wafer with four APD chips (left), ceramic endplate with pin-outs (right).

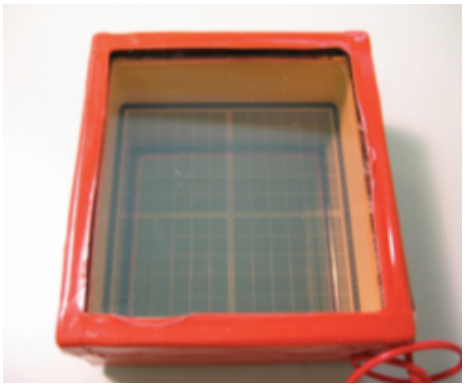


Figure 15: Hybrid Avalanche Photon Detector.

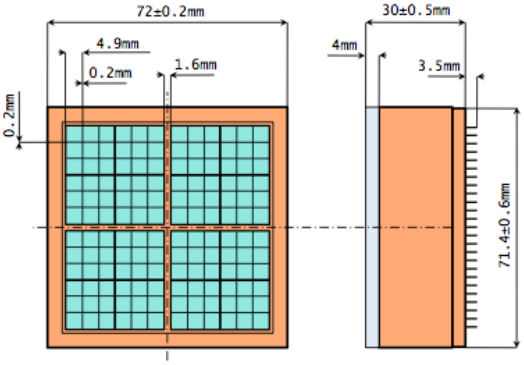


Figure 16: Hybrid Avalanche Photon Detector - detector dimensions.

Package size	72 x 72 mm^2
No. of pixels	12 x 12 (6x6/APD chip)
APD bias	about 400V
Avalanche gain	about 50
Pixel size	4.9 x 4.9 mm^2
Effective area	67%
Typical QE	25%
HV	-7kV
Bombardment gain	about 1700
Total gain	about 10^5
Pixel capacitance	80pF
S/N	15
Weight	220g

Table 1: HAPD parameters

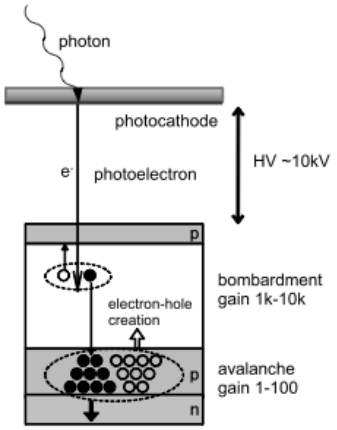


Figure 17: HAPD principle of operation.

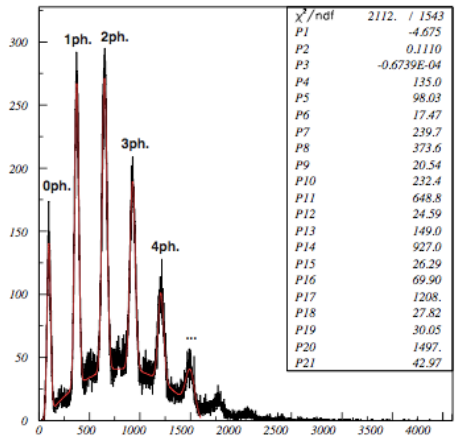


Figure 18: Hybrid Avalanche Photon Detector - pulse height distribution.

4 HAPD readout system

Much of the available space in the aerogel RICH detector is used for the expansion volume. Therefor, the complete readout system for the HAPD photon sensors has to be confined into a narrow space of a few centimeters. This poses severe space constrains for electronic readout boards and cabling. It also restricts power consumption in order to facilitate cooling of the entire device. A further constraint comes from the fact that once the system will be installed, the access would be possible only a few times during the whole 10 years of operation of the experiment. In this chapter we will discuss the electronic readout system designed to meet the requirements of operation for the Belle II aerogel RICH detector.

A typical signal from the HAPD sensor corresponds to a charge of about $5 \cdot 10^5 e_0$ and has a subnanosecond length. The front-end read-out electronics board has to:

- amplify and shape the analog signals from the hybrid avalanche photon detectors
- discriminate and digitize the amplified and shaped analog signals
- set the signal discrimination threshold
- have a very short dead time between two analog signals at the input
- enable test pulses
- enable digital signal monitoring
- enable analog signal monitoring
- enable power supply monitoring
- measure the board temperature
- provide the bias supply voltages for the HAPD
- have a low power consumption
- operate in a magnetic field of 1.5 T
- operate in a radiation environment

In the following sub-chapters the components used in the readout system for the HAPD sensor will be discussed, as well as the programs which are necessary for the operation of the system.

4.1 Hardware

Readout systems for photon sensors may be designed in different ways depending on the application. One widely used approach combines application specific integrated circuits (ASICs) with processing logic which communicates with an external data acquisition system. Typically an ASIC circuit digitizes analog signals. A dedicated processor controls the acquired data and communicates with the outer world. Along with these two major components of the readout board, a number of support circuits is needed for a proper operation. These are for example threshold voltage generators and temperature and power supply monitors. All these different systems are to be placed on a printed circuit board (PCB) of a size that would fit into the aerogel RICH detector system.

4.1.1 Applications specific integrated circuits

Building electronic circuits out of discrete components results in large devices with usually higher power consumption, low frequency response and increased noise levels. An excellent alternative are application specific integrated circuits. They allow the implementation of various electric circuits for signal treatment on a single silicon substrate. This has the advantage of reducing the size of the device, increasing the number of available channels and reducing the power consumption. ASIC systems can be customized for a specific application and made in fabric topologies which can withstand radiation. Such integrated circuits are designed in CMOS technology ranging from micrometer to nanometer technologies. Bare chips are usually packed in plastic or ceramic packages and later soldered on printed circuit boards. In applications where volume poses severe restrictions, bare chips can be bonded directly to the sensor with bond wires.

The ASIC chip for the proximity focusing RICH has been developed in a collaboration with the Japan Aerospace Exploration Agency [13]. The chips are fabricated in the 35 μm production process, packed in a low temperature co-fired ceramic package (LTCC) with a Ball Grid Array (BGA) pin-out, and measuring 13 mm $\times$ 13 mm. Each ASIC chip has 36 input channels (Fig. 19).

The readout chips were developed in several steps. In the first chip version (SA01), the analog chain consisted of an amplifier, shaper, comparator and a digital part used as a data pipeline; the pipeline was dropped from the design in later versions. More recent chip versions are SA02 and SA03 (Figs. 20, 21). The differences between them are in the architecture (SA03 is radiation hardened), shaping constants, and methods of programming [14].

Each channel of the SA02/03 chip consists of a charge sensitive preamplifier (CSA), a second order shaper (SHAPER) circuit and one bit comparator

(COMPARATOR) for digitalization (Fig. 21). The CSA works as a low pass filter with high transimpedance amplification. The voltage output of the CSA is proportional to the amount of charge collected on its input. The output of the CSA is a signal with a small rise time and an exponential decay. This signal goes into the next stage, the shaper circuit. The shaper circuit shapes the signal in a triangular shape and allows to set up the peaking time. The peaking time or shaping time (τ) is defined as the time needed for the signal to rise from 10% to 90% of its peak value. The shaped signal then enters the comparator. The comparator is simply a circuit that outputs a single-ended 1.65 V logic true signal if the analog input signal is higher then the set discrimination threshold. The presented signal path is shown in Fig. 21.

The width of the digitized signal is equal to the time the analog signal has been over the preset threshold. Below the threshold, the output of the discriminator is constantly at 1.65 V. The same threshold level is set for all channels by an external reference. Channel offsets can be set individually in 15 coarse steps of 40 mV and additionally 15 fine steps of 4 mV in order to equalize the response of the chip. The ASIC has a separate single output for monitoring signals at different stages in the front-end. These positions are marked in Fig. 22 with Vout1, Vout2 and Vout3. The amplification factor of the charge sensitive preamplifier and the shaping constant allow adjustments to optimize the signal-to-noise ratio.

The SA02 ASIC chip has two kinds of parameters: "global parameters" (Table 3) and "channel parameters" (Table 4). The former is common to all the 36 channels in the ASIC, while the latter can be set for each channel separately (Fig. 22).

The ASIC gain is illustrated in Fig. 23, where the pulse height response is plotted as a function of the input charge [15]. For low gain settings, the response is nearly linear; for the highest gain setting, however, the response of the chip tends to saturate the output signal.

To better understand the behavior of the chip, the SA02 ASIC was analyzed and the analysis of the noise will be presented below. A model of the

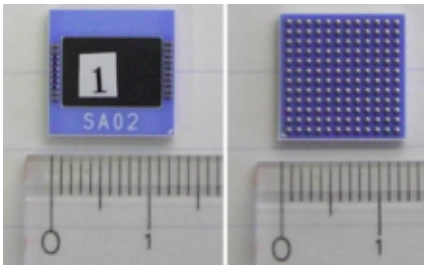


Figure 19: SA02/03 ASIC chip in the LTTC package. [14]

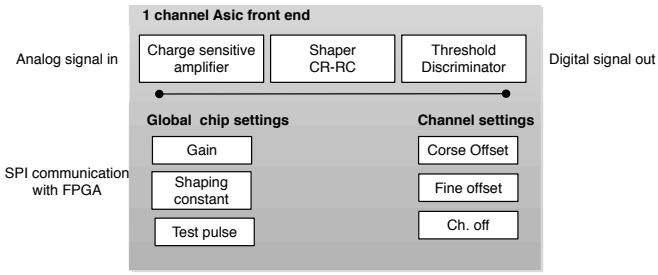


Figure 20: ASIC single channel and available settings.

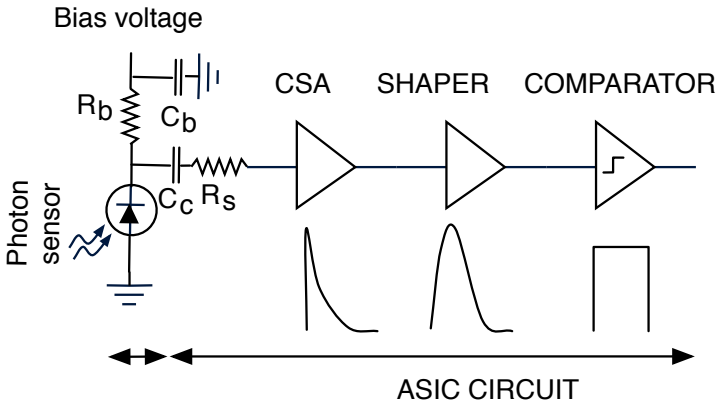


Figure 21: Schematics of the single channel of the SA02/03 ASIC.

SA02 ASIC	
Chip size	6.5 × 3 mm^2
Package size	13 ×13 mm^2
No. of channels:	36
Technology	TMSC 0.35 μm process
Standard input	60000 e$^-$
Gain	20-70 mV/fC
Shaping time	250 - 1000 ns
ADC	1 bit leading edge discriminator
Power supply	± 1.65 V
Power consumption	3.7 mW/ch

Table 2: List of parameters of the SA02 ASIC [9].

Register	Name	Function
D[1:0]	PHASECMPS	Reverse transfer capacitance for phase compensation
D[3:2]	GAIN	Gain (3=min, 0 = max)
D[5:4]	SHAPINGTIME	Time constant of the shaper (0 = min, 3 = max)
D[6]	COMPARATOR	Selection of the comparator (0 = unipol, 1 = diff)
D[14:7]	VRDRIVE	Output drive
D[16:15]	MONITOR	Select position monitor for analog signal‡
D[25:17]	ID	9 bit chip ID ; read only

Table 3: List of global parameters [14].

ASIC front-end can be described by a transfer function. The transfer function for a time invariant system is defined as the Laplace transform of the output signal over the input signal with initial conditions equal to zero. The approximated electronic circuit used in SA02 can be seen in (Fig. 22) [14].

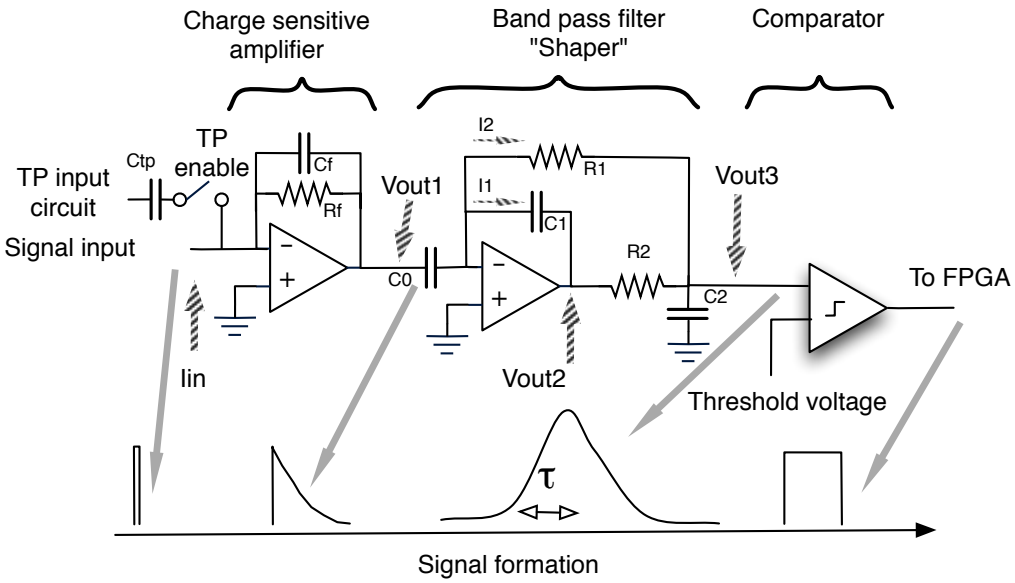


Figure 22: Signal path in the SA02 ASIC [14].

Register	Name	Function
D[2:0]	DECAY TIME	Decay time of the preamplifier (not-used)
D[6:3]	OFFSET	Coarse offset adjustment
D[10:7]	FINEADJ UNIPOL	Offset adjustment for unipolar comparator
D[14:11]	FINEADJ DIFF	Offset fine adjustment for differential comparator
D[15]	–	reserved
D[16]	TP ENABLE	Test pulse enable (1 = disable, 0 = enable)
D[17]	KILL	Disable channel (1 = disable, 0 = enable)

Table 4: List of channel parameters [14].

Equations describing the electric circuit are written in Laplace transformations. The transfer function for the charge sensitive amplifier can be derived as follows:

$$CSA(s) = \frac{V_{out1}}{I_{in}} = \frac{R_f}{sR_fC_f + 1} \ , \tag{10}$$

and the the shaper transfer function as:

$$\frac{V_{out1}}{\frac{1}{sC_0}} = -\frac{V_{out2}}{\frac{1}{sC_1}} - \frac{V_{out3}}{R_1} \ , \tag{11}$$

$$\frac{V_{out2} - V_{out3}}{R_2} = \frac{V_{out3}}{\frac{1}{sC_2}} + \frac{V_{out3}}{R_1} \ , \tag{12}$$

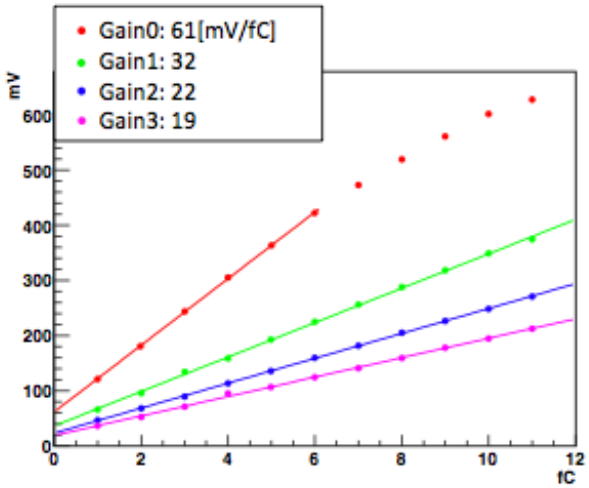


Figure 23: ASIC SA02 gain settings [15].

Combining the above equations and rearranging we arrive at:

$$V_{out3}R_2\left(\frac{1}{R_2}+\frac{1}{\frac{1}{sC_2}}+\frac{1}{R_1}\right)=V_{out2}\ , \tag{13}$$

$$\frac{V_{out3}}{V_{out1}}=\frac{sC_0R_1}{s^2C_1C_2R_1R_2+sR_1C_1(1+\frac{R_2}{R_1})+1}\ . \tag{14}$$

For the case when the value of R1 is much bigger than R2, the equation reduces to

$$Shaper(s)=\frac{V_{out3}}{V_{out1}}=\frac{sC_0R_1}{s^2C_1C_2R_1R_2+sR_1C_1+1}\ . \tag{15}$$

The transfer function of the system can be written as a product of transfer functions of the CSA and of the shaper circuit.

$$\frac{H(s)}{U(s)}=CSA(s)Shaper(s)\ . \tag{16}$$

where U(s) is the input current and H(s) is the output in Volts.

Eq. (16) can be solved numerically in Matlab, a software package for computing. The results are shown in the form of a so-called Bode diagram to present the magnitude and phase response (Fig. 24) of the system.

The behavior of the SA02 chip front-end has the character of a CR-RC^2 filter. The CR filter is determined by the 20 dB/decade rise of the amplitude response, while the RC^2 is defined by the 40 dB/decade drop. The model can be excited with an impulse response as well, and Fig. 25 displays the front-end output signal in the time domain for four different shaping times.

Component	Designator	Value
CSA		
Resistor	R_f	1 MOhm
Capacitor	C_f	0.04-0.14 pF
Shaper		
Resistor	R_1	300 Ohm
Resistor	R_2	3 Ohm
Capacitor	C_0	1.6 - 6.8 pF
Capacitor	C_1	0.4 - 1.6 pF
Capacitor	C_2	0.4 - 1.6 pF

Table 5: Values of the parameters used in the simulation

sensor bias current:	$i_{nd}^2 = 2eI_d$,
shunt resistance:	$i_{nb}^2 = \frac{4kT}{R_b}$,
series resistance:	$e_{ns}^2 = 4kTR_s$,
amplifier:	e_{an},i_{an} .

Table 6: Noise sources, see Fig. 26.

A modern detector often relies on low noise electronics, which use signal shaping technique to optimize the signal to noise ratio of the detected signal [16]. The degradation of sensors under radiation exposure tends to increase their leaking current. A front-end electronics with a variable shaping time can provide a tool to optimize the signal-to-noise ratio over the years of the detector operation. Fig. 26 shows an equivalent circuit of the sensor and front-end electronics.

The noise level of the detector is a combination of the current and voltage sources. The resistor R_b (Fig. 22) biasing the detector acts as a current noise source because it effectively shunts the input of the amplifier. The thermal velocity fluctuations of the charge carries from R_b pass to the ground via C_b creating a current i_{nb} (Fig. 26). Fluctuations due to electron emissions within the semiconductor detector create a leakage current i_{nd} (Fig. 26) and represent a current noise source in parallel with the sensor capacitance C_d. The resistance in series R_s acts as a voltage noise contribution. The equation array in Table 6 summarizes the noise sources.

The noise contributions are random and uncorrelated, so that they can be added in quadrature. In order to calculate the total noise at the output of a shaper circuit one has to integrate the result over the bandwidth of the shaper response. The equivalent noise charge (ENC) is the quantity of charge produced by a signal equivalent to the RMS value of noise. For an CR-RC^2 shaper with a semi Gaussian pulse shape, the ENC is described in units of

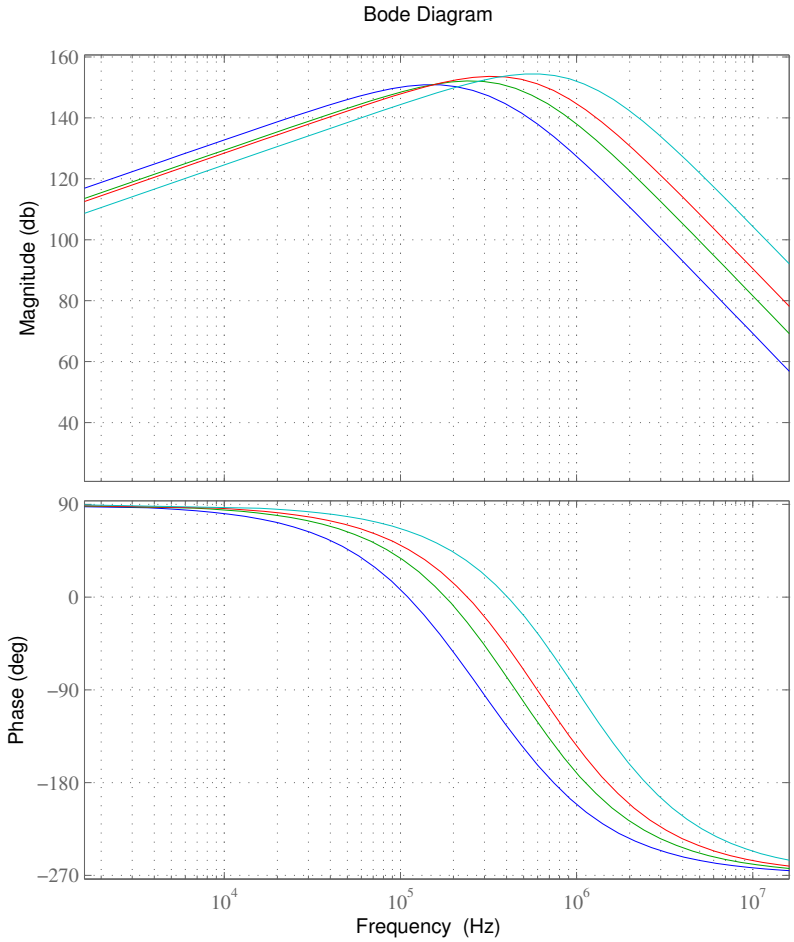


Figure 24: ASIC front-end Bode diagram for different shaping constants. Diagrams for magnitude and phase response.

electric charge:

$$ENC^2 = \frac{e^2}{8}\left[(2eI_d + \frac{4kT}{R_b} + i_{na}^2)\cdot\tau + (4kTR_s + e_{na}^2))\cdot\frac{C_d^2}{\tau} + 4A_fC_d^2\right] . \tag{17}$$

The elementary charge is denoted with e, I_d represents the sensor bias current, k is the Boltzmann constant, T is the absolute temperature in Kelvin, and τ is the shaping time constant of the shaper circuit. The amplifier voltage noise power density e_{na} is of the order of few $\mathrm{nV}/\sqrt{Hz}$, and current noise power density i_{na} ranges between $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ and $\mathrm{fA}/\sqrt{\mathrm{Hz}}$, depending on the technology used in the production.

To estimate the HAPD ENC we assume that the sensor initial leakage

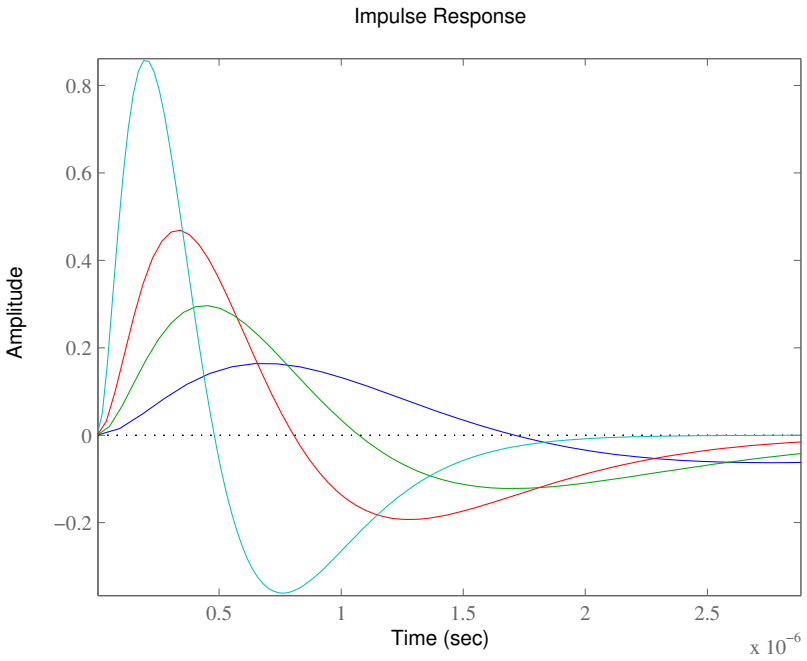


Figure 25: ASIC front-end response to a single photon equivalent charge with different shaping constants. Amplitude response [V] in time domain.

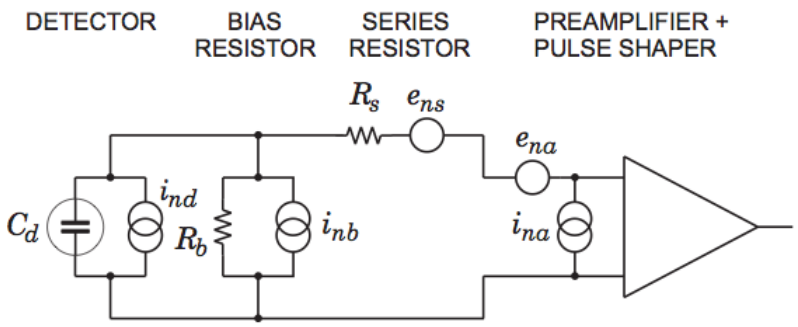


Figure 26: front-end and detector equivalent circuit for noise analysis [16].

current is about 30 nA per pixel. The leakage current of the HAPD will increase during the operation due to radiation damage by a factor of about 20 and after 10 years operation will be around 600 nA to μA per pixel [9]. The resulting equivalent noise charge for the HAPD sensor in units of elementary charge as a function of peaking time is shown in Fig. 27.

The shaping time allows us to find a balance between current and voltage sources of noise. Voltage noise increases by shortening the shaping time, while current noise is dominant at larger shaping time. For a non-irradiated HAPD the noise level is expected to be around 1200 e^- at 80 pF of capacitance. A

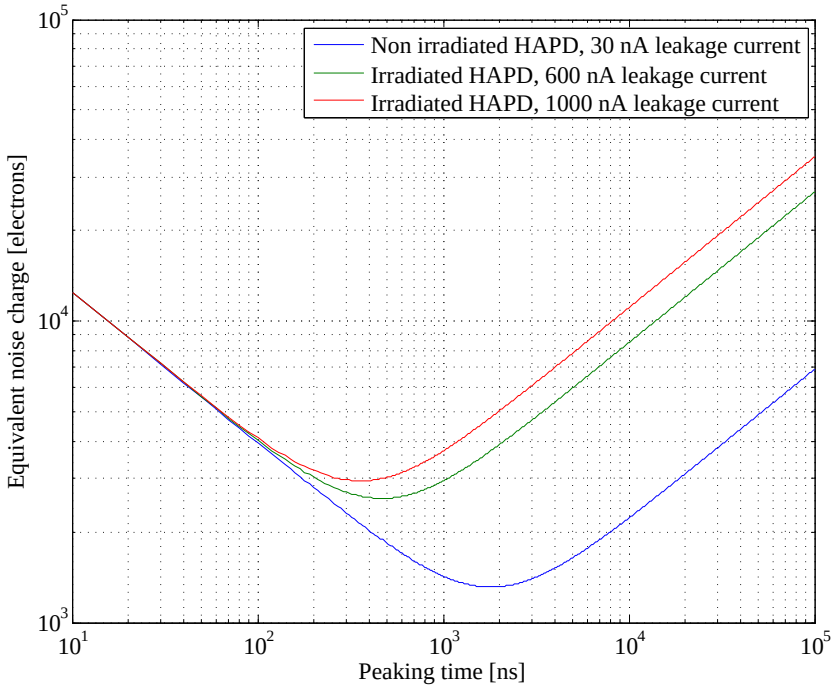


Figure 27: Equivalent noise charge as a function of peaking time for a non irradiated and irradiated HAPD.

suitably chosen shaping time range can help keeping a constant detection efficiency during the experiment life span.

4.1.2 Field programmable gate array

Field programmable gate arrays (FPGAs) are re-programmable electronic circuits [17]. Due to their computing power and versatility they are widely used in various systems, specifically where large amounts of data needs to be processed in real time. Areas of their application include radio frequency receivers, radar systems, positron emission tomography scanners, measurement equipment,radiation detectors and other equipment.

The most important difference between standard processors with a fixed architecture and FPGAs is in the internal structure. Processors for their operation use command and data lines, registers, program counters, stacks, accumulator units, etc. A program for a processor can be compiled and run with a program written in the C language for example, but any operation would need to go through a fixed architecture. Contrary to this approach an FPGA allows to create an internal architecture by the user, called also system-on-chip (SoC) design. Moreover, the architecture can be altered by rewriting the program. The user has thus the possibility to create a unique digital logic design that best suits its application. This approach has another advantage. The overall functionality of the device can be altered without any hardware modification. FPGAs are programmed using a Hardware Descriptive Language (HDL). This language allows to describe binary operations.

FPGAs are programmable semiconductor devices that are based on a matrix of Configurable Logic Blocks (CLBs) (Fig. 29) connected through programmable interconnects [17]. The CLB is the basic logic unit in a FPGA and is composed of two slices. Each slice consists of a lookup table, a flip-flop and connections to outer cells. FPGAs also include small portions of block random access memory (BRAM) which can be used for a local storage of data. When programming an FPGA, the automatic synthesis of the VHDL file creates connections between CLBs and fills the lookup tables in order to assign a predefined operation. This is called firmware.

Once the internal architecture is defined, the signals enter and exit the FPGA via inputs and outputs (IOs). Some IOs have specific functions. These are for example connections for loading the firmware into the FPGA, or a clock buffered pin which distributes the clock to the chip; some IOs are used as hardware boot up sequence definers. Most of the IOs are arranged in banks. A bank is a subset of IOs that work on the same voltage level. FPGAs come in several different physical packages.

Certainly the least space consuming is the ball grid array option (BGA) in Fig. 28 as the IOs and power pins are arranged in a matrix below the chip. The choice of the device to be used in the front-end was driven by the mechanical chip size, IOs to interconnect the ASICs and other components and the size of the logic. We have chosen the Xilinx Spartan6 XC6SLX45. Table 7 summarizes the device.

Package size	BGA FGG484 23×23 mm
No. of IOs	316
Logic cells	43,661
Distributed RAM	116×16 Kb size
IO banks	4

Table 7: Spartan 6 XC6SLX technical specification [17].

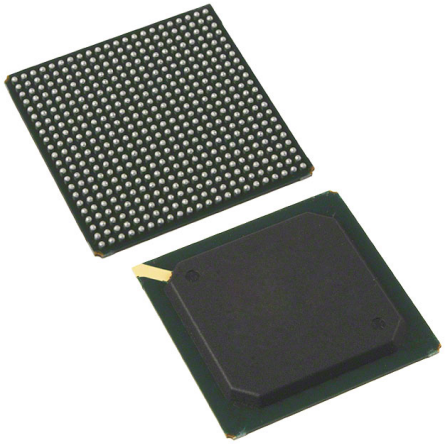


Figure 28: Image of Spartan 6 device in BGA package [17].

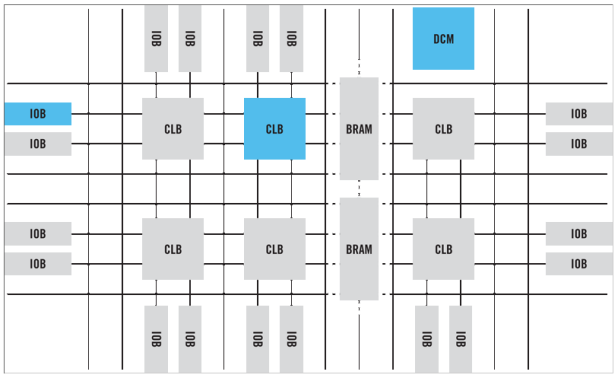


Figure 29: FPGA structure showing the matrix interconnection of CLB, BRAM and IOs [17].

In what follows, the hardware components of the readout board which support operation during data measurements will be described.

4.1.3 Threshold voltage circuit

ASIC chips need a threshold voltage for signal discrimination. A device that sets a threshold discrimination level for the ASICs is composed of commercially available components (Fig. 30) and will allow to set a threshold voltage V_{th} in the range from -1.25 V to 1.25 V with a resolution of 2.5 mV.

- a voltage reference diode of V_{ref} 1.25 V - ADR1581[18],
- a 10 bit, 2 channel potentiometer - AD5235 [19],
- an operational amplifier - LM8262 [20]

The voltage output of the device is proportional to the 10 bit value of the potentiometer and calculated using:

$$V_{th} = \frac{2 \cdot \mathrm{V}_{ref}}{\text{range}} \cdot \text{Data} - 1.25 \text{ V} , \tag{18}$$

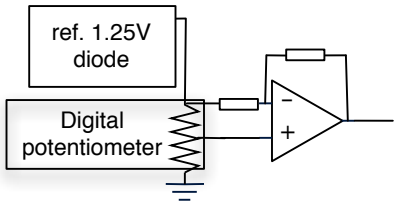


Figure 30: Threshold circuit diagram, resistors have a value of 100 kOhm.

4.1.4 Selection of the monitoring signals

The possibility to monitor remotely the ASICs internal signals and power lines of the readout system gives the possibility to debug and test the operation of the readout electronics. The system allows to monitor the internal signals (of the four ASICs on board) for each channel along the front-end chain. It also allows to monitor the threshold voltages and power supply voltages. The routing device consists of a dual 4-channel analog multiplexer/demultiplexer ST M74HC4052 [21]. The device was primarily chosen because it has a small series resistance of 7 Ohm and a large enough band width to route analog signals without degradation. The signals from the board are routed to a connector on the readout board.

Table 8 and Fig. 31 describe its functionality.

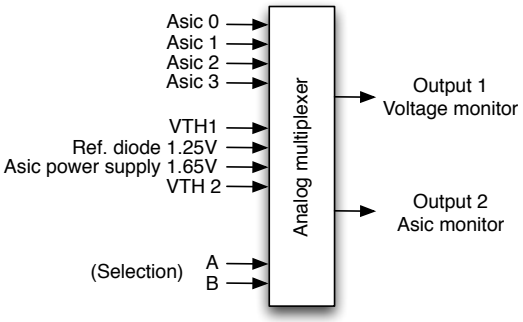


Figure 31: Analog signal multiplexer. By setting two bits A and B both outputs 1 an 2 are selected but not independently.

4.1.5 Temperature monitors

The measurement of temperature is provided by two temperature sensors. One of the possibilities is to use the TMP121 by Texas Instruments which offers the temperature monitoring with an accuracy of 1.5 °C within the range from -25 °C to 85°C in a small package [22]. The chip has an internal temperature sensor, a digitalization unit and a shift register. Temperature is decoded from the 12 bit value and one polarity bit

Selection	Output 1	Output 1
B A bits	Monitor of the board voltages	Analog output monitor of the SA02 ASIC
0 0	V_{th}	ASIC 1
0 1	Reference diode 1.25 V	ASIC 3
1 0	ASIC power supply 1.65 V	ASIC 0
1 1	V_{th2}	ASIC 2

Table 8: Multiplexer parameters

$(Pol = 0(T > 0°C)\ and\ Pol = 1\ (T < 0°C))$. On request, the chip sends a 16 bit frame with the last measurement (Fig. 32) [22].

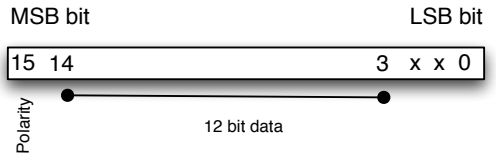


Figure 32: Temperature reading register.

The temperature is calculated as :

$$T = \text{Polarity} \cdot 0.0078\ [°\text{C}]\ \cdot \text{Data}\ . \tag{19}$$

4.1.6 Test pulse

The test pulse circuit injects charge into the ASICS inputs. The circuit is primarily intended for verifying the correct response of the ASICs front-end. The charge injection circuit is composed of two adjustable voltage sources AD5235 [19] and a switch ADG779 [23] that flips between them (Fig. 33) within few ns. It is thus possible to inject a controlled amount of charge into the front-end of every channel and remotely observe the response. The charge injection pin on the ASIC is common for all channels. Activating the circuit sends a voltage step toward the ASICs Fig. 34.

The charge injected is calculated using the equation:

$$\Delta Q = \Delta \text{V} \cdot \text{C}_{tp}\ . \tag{20}$$

The capacitor C_{tp} on the input (Fig. 22) of the front-end chip has a value of 0.1 pF. A voltage step of about 100 mV will inject $\approx$ 10 fC of charge into the front-end of the ASIC chip. The charge corresponds to about 60000 e^-.

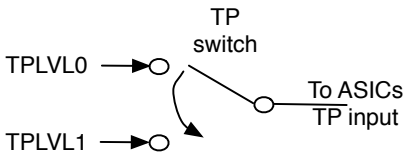


Figure 33: Test pulse circuit.

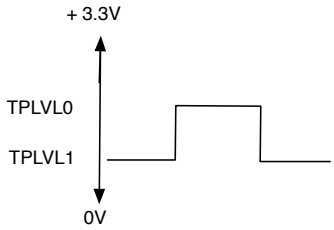


Figure 34: Test pulse circuit output.

4.1.7 Readout electronic board

The above mentioned electronic components should fit onto a single printed circuit (PCB) board (Fig. 35)

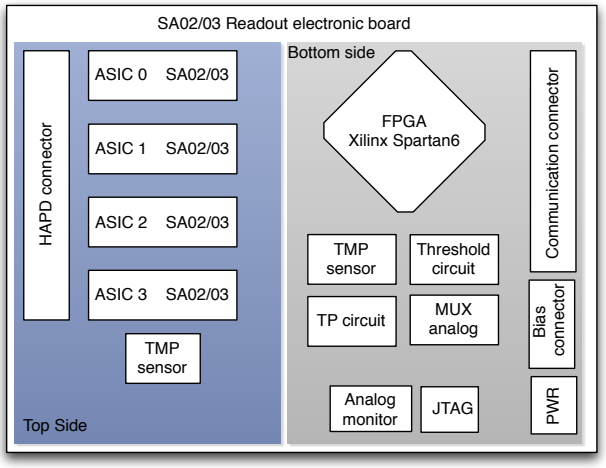


Figure 35: SA02 readout board functional description.

The readout board has on one side a multi pin connector for the HAPD sensor, a temperature monitor and four ASIC chips for signal digitalization. On the other side it has the FPGA chip, threshold circuitry, temperature monitor, test pulse system and the analog multiplexer. It also has two connectors for power supply and HAPD bias connection. A dedicated programming connector is used to program the FPGA and two 64 pin connectors are used to connect an extension board.

The board was designed in Altium Designer [26]. First the connections were drawn between the components in design schematics. The PCB components and their connections were than made by using the schematics. Due to many interconnections the board was routed manually.

The PCB board has multiple layers for analog and digital tracks which guide the electric signals between chips and connectors. In order to minimize the crosstalk of digital signals into the analog signal path lines, ground layers

are placed in between. Additional layers serve for power supply distribution and for the HAPD bias supply. The result is a 12 layer mixed signal (digital and analog signals) board with the minimal distance between two tracks of 0.254 mm. The 12 layer board is produced in several steps, since some layer interconnections do not go through all layers. The solution was found to make a design with two boards having 6 layers each. Then the two 6 layer stack boards are put together and the missing connections are added. That needs to be made to avoid an even more complicated procedure of making buried-in vias (Fig. 36). As a result a complex 12 layer PCB board is made.

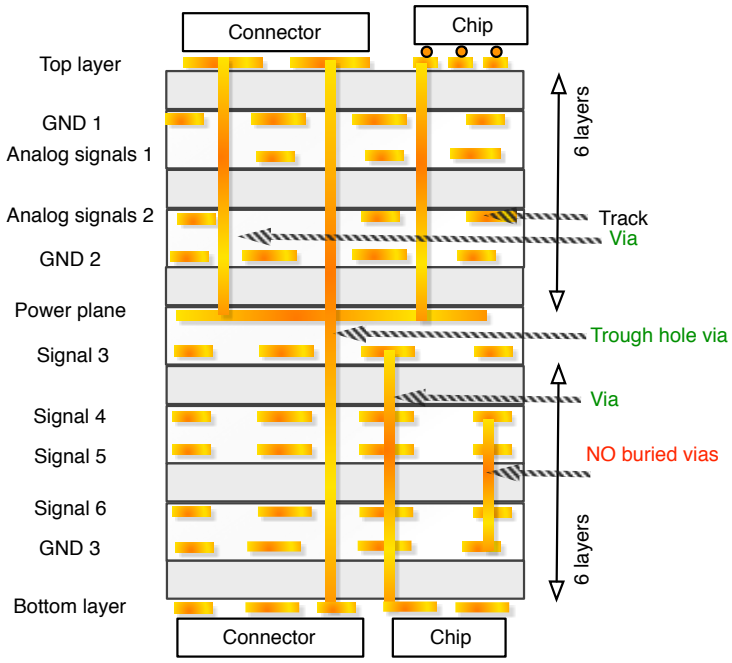


Figure 36: SA02/03 PCB stack layers.

This procedure considerably simplifies the production of the board. Figures of the internal PCB layers are shown in the appendices. The front-end board is shown in Figs. 37 , 38.

The very first initial tests included the measurements of power consumption as this would be the very first indicator of potential problems. The SA02 ASIC chip needs the power supplies as summarized in Table 9.

The four ASIC chips consume about 112 mA on positive rails and 190 mA on negative rails. The total power consumption per board amounts to about 0.65 W. Initially, simple testes were done to verify the correct operation of the FPGA, verify the 48 MHz on-board clock and measure the leaking current of the bias supply voltages. All tests show results as expected.

In addition to the front-end board, another interface board was developed [24]. This board serves as an extension to the readout board (Fig. 39)

Pin	Power line	Value
1	VSS	-1.65 V (ASIC analog)
2	VDD	1.65 V (ASIC analog)
3	VDD1	1.65 V (ASIC digital)
4	VSS1	-1.65 V (ASIC digital)
5	VCCINT	1.2 V
6	VCCAUX	2.5 V
7	VDD33	3.3 V
8	none	
9	VDD15	1.5 V
10	DGND	Digital ground
11	AGND	Analog ground

Table 9: Power supply connector description.

and has a programmable read only memory (PROM) chip to start the FPGA. The PROM is necessary to load the program on the FPGA at every power up in order to avoid the firmware loading from a computer. An Ethernet controller with a corresponding connector allows the integration of the front-end board in a local computer network (Fig. 40). Two dual in-line connectors allow connection of the readout board to an external system using a 34 pin twisted pair flat cable with freely programmable IOs available for communication interface (Fig. 41). Analog signals from the readout board are routed to four MMT RF connectors.

Fig. 42 shows the photon detection module consisting of the HAPD, the

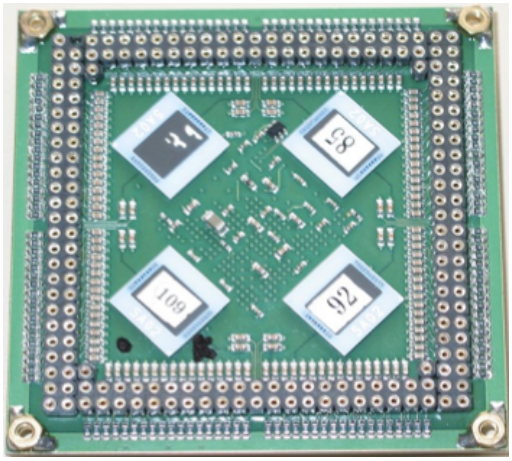


Figure 37: SA02 board top side (HAPD connector).

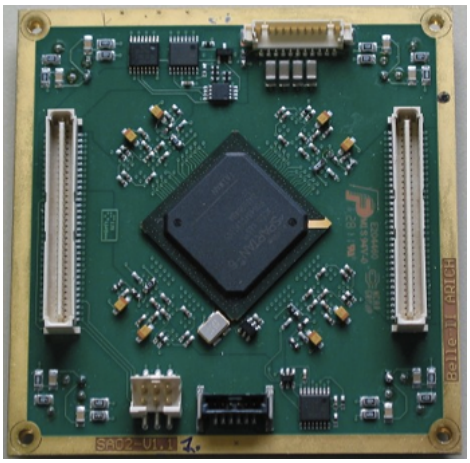


Figure 38: SA02 board bottom side (service connectors).

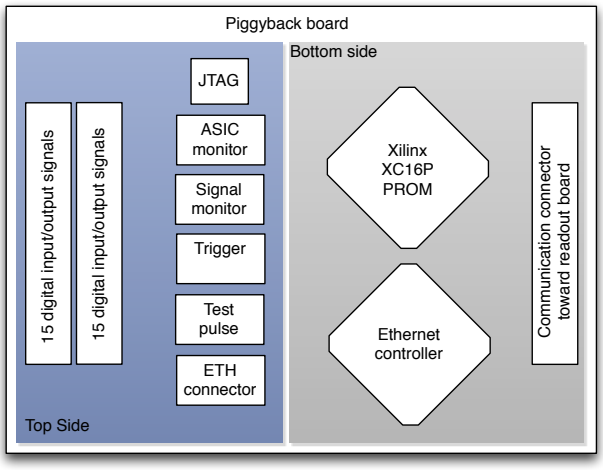


Figure 39: Interface board functional description.

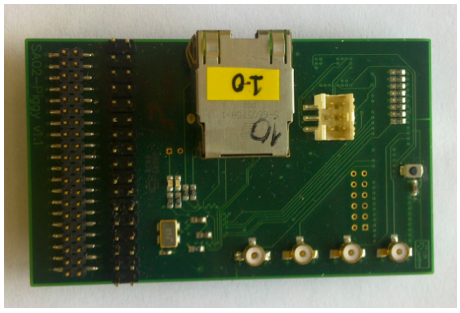


Figure 40: Interface board bottom side.

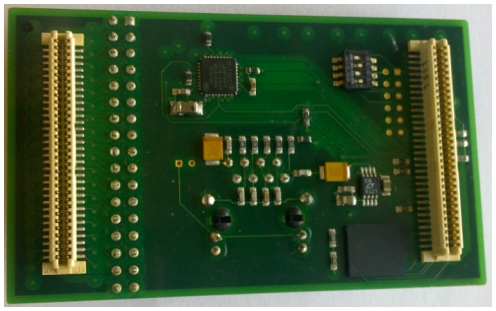


Figure 41: Interface board top side, connection to the readout board.

front-end board and interface board.

Figure 42: HAPD sensor, front-end board and interface boar.

4.2 Firmware

An FPGA needs a firmware for operation. The firmware design for the readout board is subdivided in a processor that controls the board and a readout part that acquires and process data (Fig. 121). The firmware is built in a vendor specific environment. Within the programming environment some precompiled code is available called Intellectual Property (IP) cores for various applications. I have used two IP cores: the clock management system and a soft error mitigation controller. The clock management system is a core that generates clocks of different frequencies based on the input clock. It distributes the clocks inside the FPGA to minimize internal clock skew or delays. The second core, the Soft Error Mitigation (SEM) controller, allows to monitor potential firmware errors in the FPGA during operation. First, the processor will be described, followed by the readout an used IP cores.

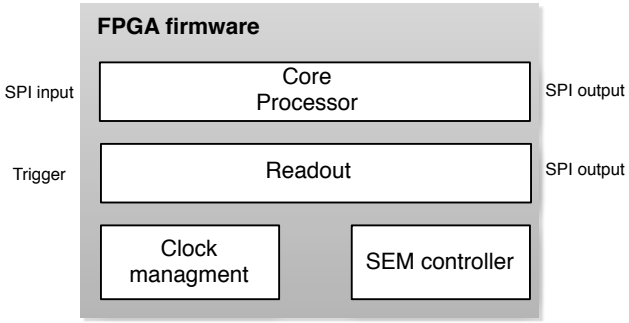


Figure 43: FPGA firmware (SA02 core) block diagram.

4.2.1 Processor

The front-end electronic board is composed of multiple devices and needs a control mechanism in order to allow the correct operation and control of the readout system.

A simple and elegant way to make a unified system to control devices is a custom processor for different hardware and software devices. Its purpose is to control different components with a reduced list of commands. This is particularly useful as the user addresses each peripheral device directly. A device can either be a hardware chip, threshold setting for example, or a parameter that sets the operation inside the readout system. The complete list of instructions can be found in the appendices. The processor is composed of some major circuits, a receiver, a sender, a controller and drivers. The processor uses a simplified version of a Serial Protocol Interface (SPI) for communication (Fig. 44). This is a 3 wire protocol that allows a connection between the electronic circuits in a master slave configuration. The frame

signal indicates that the transmission is active. At the clock rising edge, data bits are transmitted from registers of one system into another.

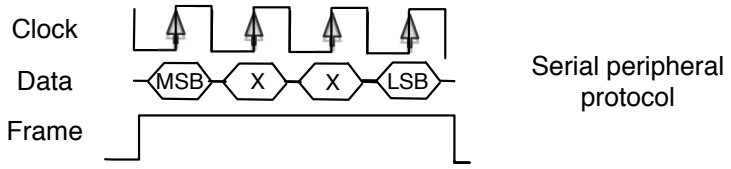


Figure 44: SPI communication protocol example for a 4 bit transmission showing the correct clock polarity.

The processor is programmed via an 64 bit frame (Fig. 45) sent over SPI bus. When sending the frame, the most significant bit (MSB) must be sent first toward the SA02 processor. The first 8 bits (63 to 56) are used to address the device on the front-end board. Bits from 54 to 8 are used to send data while bits 7 to 0 are unused but necessary for correct transmission.

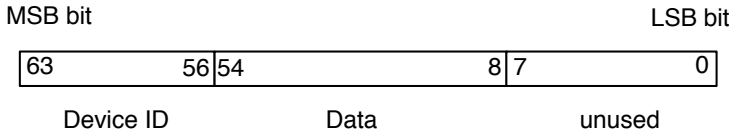


Figure 45: Input frame, bit setting.

The receiver of the processor is preconfigured in a slave mode. This means that the processor itself can be accessed at any time and will reply immediately through the SPI output, which is in the master mode. Essentially this is a full handshake communication for most of the messages, some however do not foresee a reply. The FPGA operates with his own internal clocks and a message coming from outside is not synchronized. This means that an asynchronous transmission needs to be synchronized first in order to be executed.

The procedure for writing into a processor is as follows (Fig. 46). A receiving frame through a state transition in the receiver circuit. When the full frame has been transmitted, the receiver notifies the controller via an execute signal that a new command needs to be executed. The controller identifies the ID of the device being addressed and activates the correct driver for the request. In case the frame is not valid or the ID of the device is unknown, no operation is triggered. When writing to threshold settings, ASICs or temperature monitors, the last stored data are transferred back. The sender circuit collects the read back information from the devices and sends them via a separate SPI bus to the external system. The processor commands are listed in Appendix C.

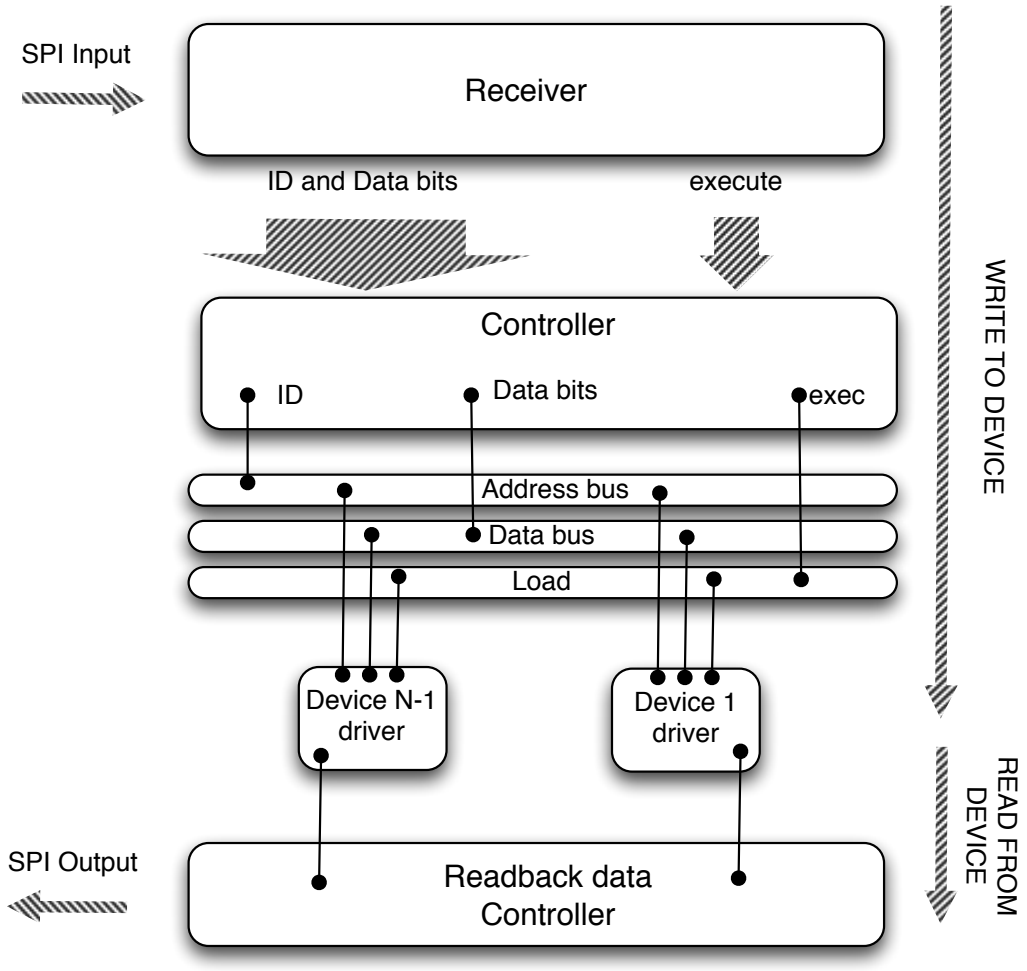


Figure 46: Processor execution routine.

There is a limitation that should be noted. There should be at least 500 μs between two transmitted frames to allow the drivers loading and reading devices, but this does not affect much the measurement operation as the processor manages only the slow control processes. The processor represents a very simple and yet effective algorithm which does not consume substantially the FPGA resources, and it proved to be very reliable. It allows to set-up the front-end board. A dedicated communication line for the processor settings provide an access to the parameters without disturbing readout of the data.

4.2.2 Data readout

The second part of the firmware consists of the readout system (Fig. 47). The requirements for the proximity focusing RICH are to be able to read data at a trigger rate of 30 kHz and be able to separate two events being 250 ns apart.

The readout system can be configured in three different modes of operation with a few parameters which allow its fine tuning and facilitate the integration in a variety of test set-ups. The readout system is activated automatically at trigger event and sends acquired data via a dedicated SPI bus. The data frame is composed of 8 bits per channel separated by a control bit (Fig. 48). The content of data depends on the chosen detection algorithm and is explained in the following subsections. Control bits in the data frame can be used to monitor the transmission and should always have a zero value. In case of a transmission error it is likely that one out of 144 control bits would flip its state. The data frame transmitted via SPI bus will have the

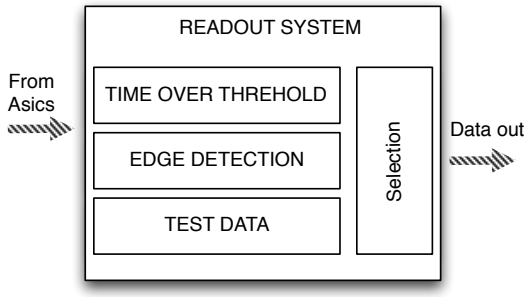


Figure 47: Readout system.

structure shown in Fig. 48.

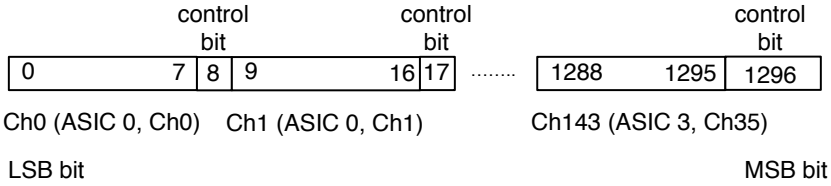


Figure 48: Readout data frame.

The available readout methods in the present read-out system are the signal rising edge (EDGE) detection, time over threshold (TOT) detection and TEST mode with a fixed data pattern. The fixed data pattern is a diagnostic tool to verify the transmission. In the readout system each input channel has a shifting register of 16 bit length where the sampled signal is recorded. The shifting frequency (or signal propagation velocity), can be adjusted globally for all channels. Each channel also has an 8 bit register

where the acquired data are stored prior to transmission. Data can be sent at different rates in dependence of the sending clock. The trigger is delayed for 10 clock shifting cycles before the transmission is activated. This allows the synchronization of the trigger with the data. Within the readout system a global parameter called 'Position' is used to determine which portion of the 16 bit register will be copied into the 8 bit register and sent to the user once the trigger was received. Figure 49 summarizes the transmission process.

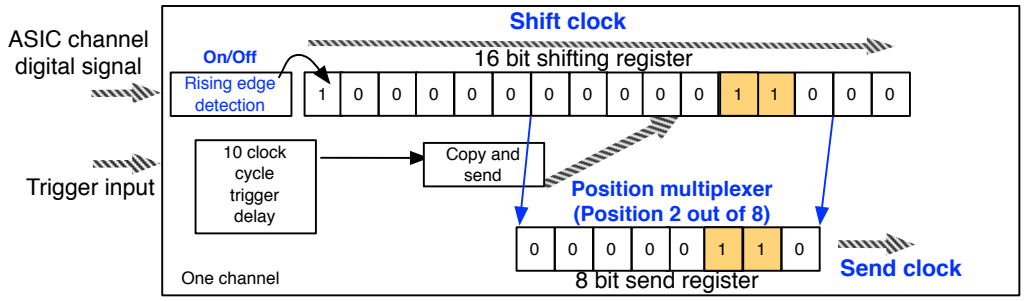


Figure 49: The data sampling and transmission.

For the edge detection algorithm, an additional rising edge detection module is enabled (Fig. 50) between the ASIC and the shift register. The mechanism detecting the edge is based on a D type flip-flop with a clock frequency of 120 MHz. This creates an internal signal with the duration of 1 clock cycle which goes into a state machine synchronized with the selected shifting clock. This state machine outputs two consecutive bits into the shift register and returns into the idle state to repeat the process at the next event. Regardless of the duration of the ASIC signal the result will be recorded as a single event.

The firmware offers also a test mode in which the fixed data patterns 0x4D is transmitted to the output bus.

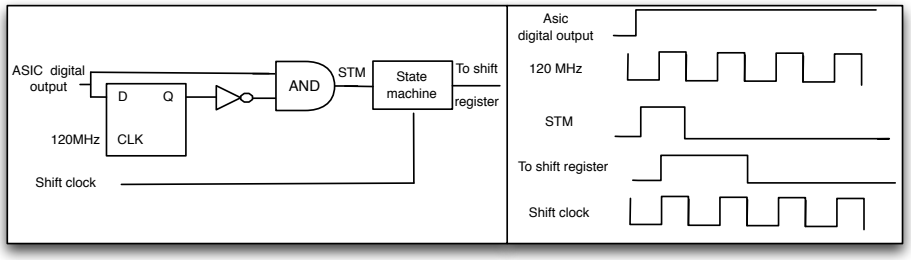


Figure 50: Edge detection principle.

The shift clock and send clock share the same setting value (Table 10). Shift clock is chosen accordingly to the ASIC shaping time. Send clock is set to a transmission frequency of 120 MHz if proper quality cable is used and

Setting	Value [MHz]
0	48
1	24
2	12
3	6
4	4
5	120

Table 10: Frequency settings for send clock and shift clock parameters.

the transmission line is correctly terminated. At 120 MHz, the data frame consisting of 1296 bits is transmitted in 11 μs.

A photon counting detector can be read by counting events produced by signals above the threshold level. By varying the threshold level, a threshold scan is obtained. This scan records the number of detected events at a certain threshold value for a requested number of triggers, and thus shows the number of acquired events in function of the threshold voltage.

A threshold scan from the time-over-threshold detection principle should look like the one shown in Fig. 51.

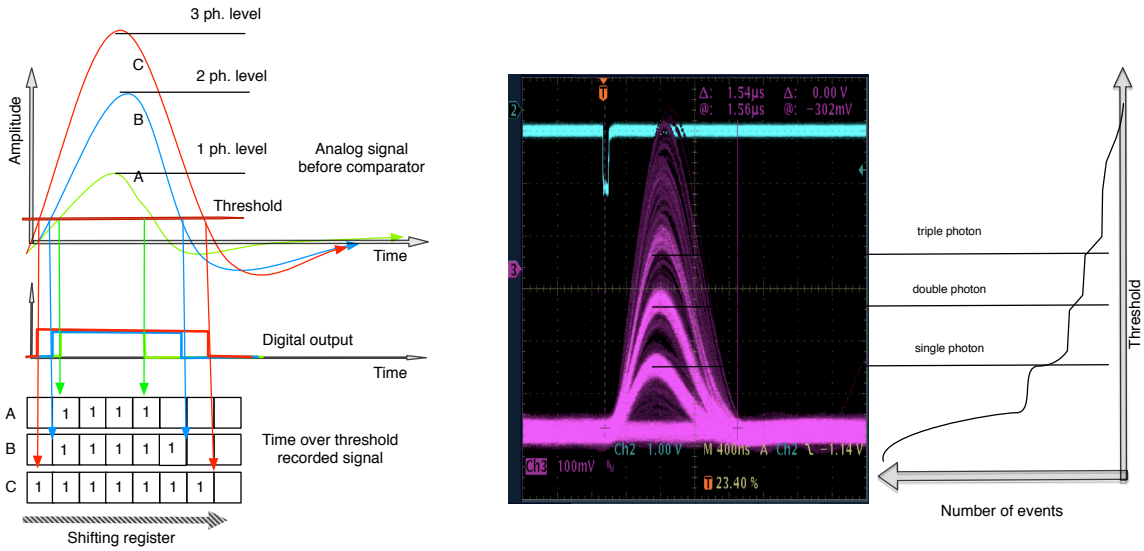


Figure 51: Time over threshold detection principle and threshold scan.

The edge detection algorithm should only record a transition of the analog signal over the preset threshold value. In this case an expected threshold scan should look like in Fig. 52.

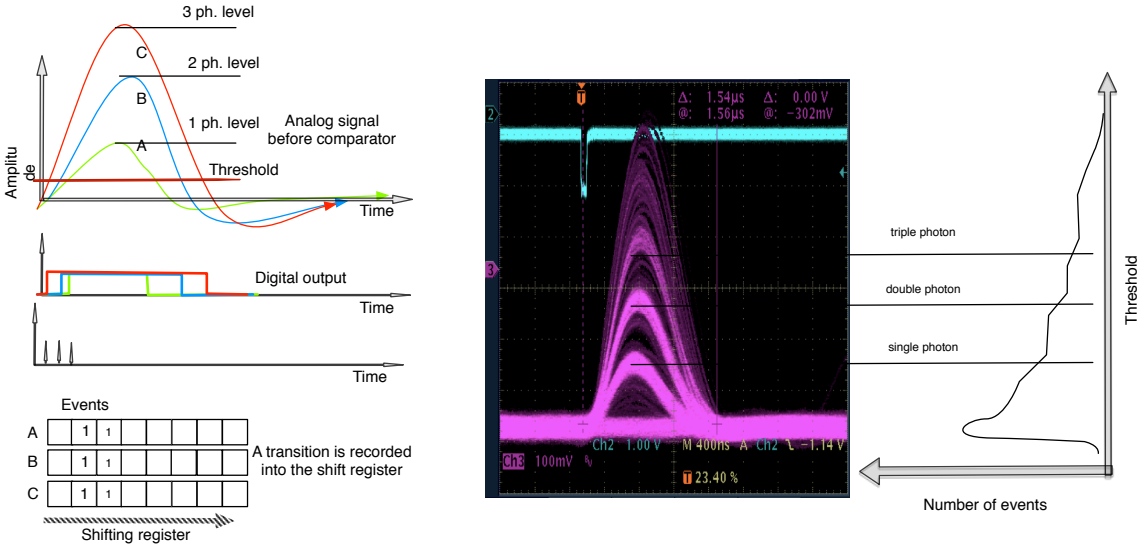


Figure 52: Edge detection principle and threshold scan.

4.2.3 Clock management and Soft error mitigation controller

Clock management in FPGAs represents a very important aspect of its reliable operation. Xilinx provides an IP core which accepts a master clock provided by an external resonator over a dedicated pin. The function of this core is to multiply or divide the master clock frequency and distribute it evenly through the device. It also spreads the internal clocking of the FPGA with a phase locked loop controlled clock that makes the device more robust to drifts of the reference clock. A precompiled clocking system provided by the vendor reduces the risk of faulty operation due to clock delays within the circuit. By including an clock management system, the compiler automatically identifies the clock paths and optimizes the latency of the clock distribution.

The last part of the firmware is the single event mitigation (SEM) controller. Ionizing radiation is capable of inducing undesired effects in silicon devices. Single event upsets (SEUs) are random, unintentional changes in the state of memory cells and can affect ASICs and FPGAs. The single event mitigation controller provides SEU detection, correction, and a classification of errors. The SEM controller does not prevent soft errors; it provides, however, a method to better manage the system-level effects of soft errors. The SEM controller:

- provides detection of events with the maximum latency of 25 ms,
- provides a serial data for port reporting status and errors,
- increases FPGA uptime by providing informations needed to decide if a firmware reload is necessary,

- allows a partial self correction of single errors.

The presented firmware together with the hardware results in a small and fully functional readout board for the HAPD photon sensor. The major advantage of a modular design approach is that the processor part can be reused in different configurations. In order to verify the operation of the readout board, a data acquisition based on the IO register was set up.

4.3 Acquisition of the data from the readout board

For laboratory measurements, a data acquisition system based on the VME system was used. The electronics board was connected to the VME system via twisted pair cables using the low voltage differential signal (LVDS) standard. The VME system is composed of a chassis, a power supply and an extension bus which accepts VME cards. A VME controller is used to connect the VME system to the computer [27].

As the VME communication module we have used CAEN V1495 [28], a general purpose VME input/output electronic board. It is based on two FPGAs, where the first one has a dedicated firmware which serves to access the VME bus, while the second is dedicated to the users to build their own algorithms. The user FPGA was programmed with a firmware that allows to communicate with the front-end board (Fig. 125).

The firmware consists of:

- A processor which translates the commands from the computer which load the SA02 readout board.
- A veto/event decision logic which ensures that new events are accepted for acquisition after the data are read or the acquisition is reset.
- The readout buffer, a serial receiver of acquired data that maps the received data to the VME bus and notifies the veto system that a new event is ready for acquisition.

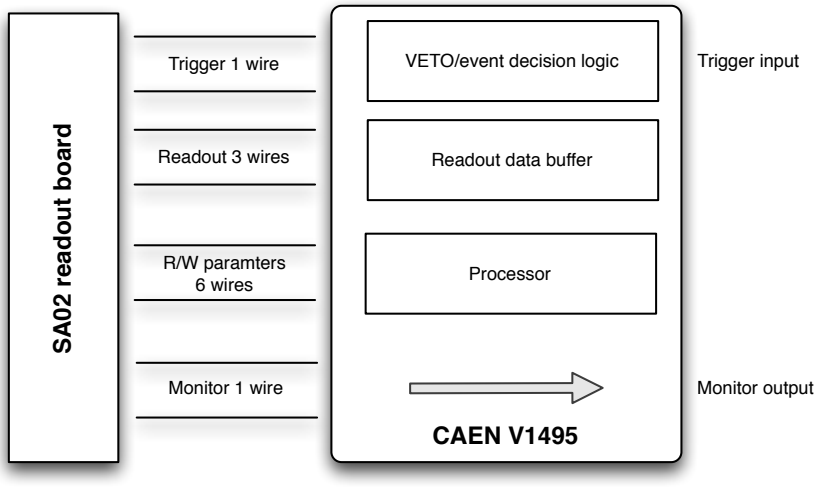


Figure 53: CAEN firmware schematic.

In order to program the front-end board, the CAEN V1495 is accessed from the DAQ system using five 32 bit registers. Two addresses are used to

write in the content to be sent to the front-end board, and one to activate the execution. The remaining address is used for reading the messages from the front-end board (Appendix E).

The block of data transmitted from the front-end board at trigger event is first fed into a serial-to-parallel register. From the data package, control bits are excluded and the recorded values are mirrored in 36 subsequent registers, each 32bit long. Given a limited number of inputs and outputs on the CAEN VME board, a wiring system was found that can accommodate up to 4 readout front-end readout boards per one CAEN V1495 board, but multiple boards can be added in the VME system. A detailed wiring diagram can be found in the Appendix D. The system for communication and signal readout of the HAPD sensor is schematically shown in (Fig. 54).

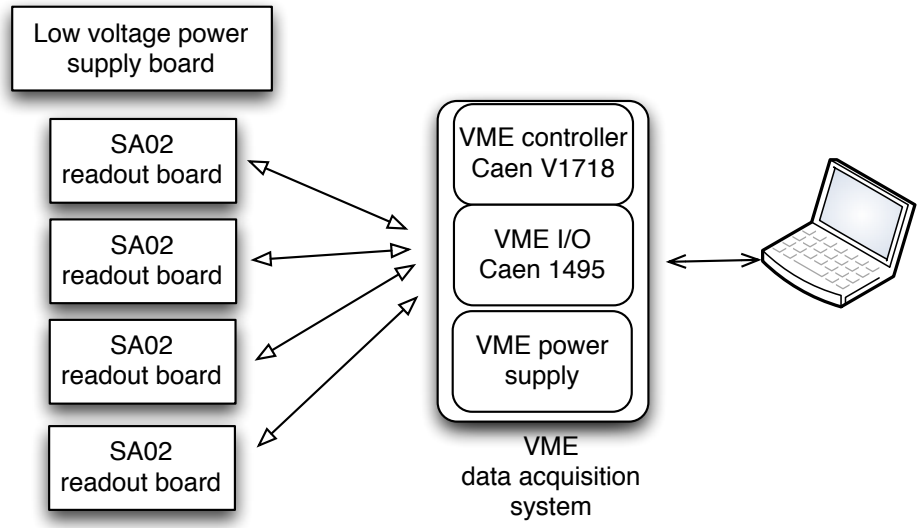


Figure 54: Main components of the laboratory set-up.

On the computer that controls the measurement, a program written in the C language loads the settings and acquires the data. Data analysis and graphical representations are done using the ROOT data analysis framework, an object-oriented C++ analysis package.

In the final design for the Belle II experiment, the VME port will be replaced with a merger boards, which will be connected on one side to 4-6 front-end readout boards, and on the other to the Belle II readout system via optical cables [15].

The merger board is based on the Virtex5 chip from Xilinx. In comparison to the Spartan 6 chip which we employ on the read-out board, it offers a larger number of IOs and available logic. The board will collect data from several readout boards and act as a pre-buffer of data. This will allow multiple triggers to choose a set of measurements from a defined event

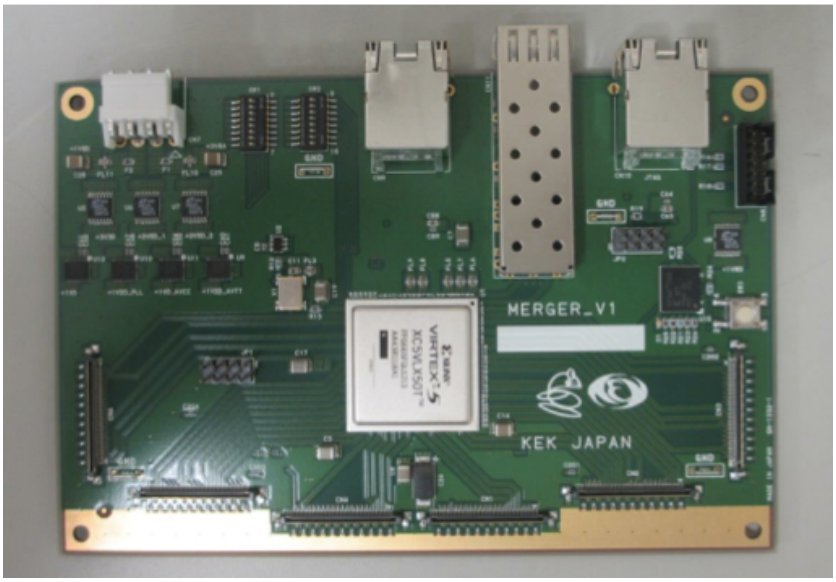


Figure 55: Merger board

time line. Additional functionality may allow the construction of an ARICH trigger system. The merger board will also provide some of the slow control operations such as loading of the firmware and firmware integrity verification of the readout boards.

5 Laboratory measurements

A newly designed system needs to be analyzed to verify correct operation. The subsystems are first tested separately, before being integrated in as the final system. The laboratory environment the initial test of the board can be made using the test equipment such as oscilloscopes, logic analyzers, voltmeters. Once the communication between the front-end board and the data acquisition system was established, the operation of the front-end board was verified by separately testing the hardware and the firmware.

5.1 Test of the peripheral devices of the front-end readout board

During the first test the threshold circuitry (Section 4.1.3) was tested in order to confirm its linearity. The output voltage range from -1.25 V to 1.25 V is subdivided into 1024 steps. The response of the threshold circuitry is linear without any fluctuations due to noise. The measured output voltage as a function of the set value of a digital potentiometer is shown in Fig. 56.

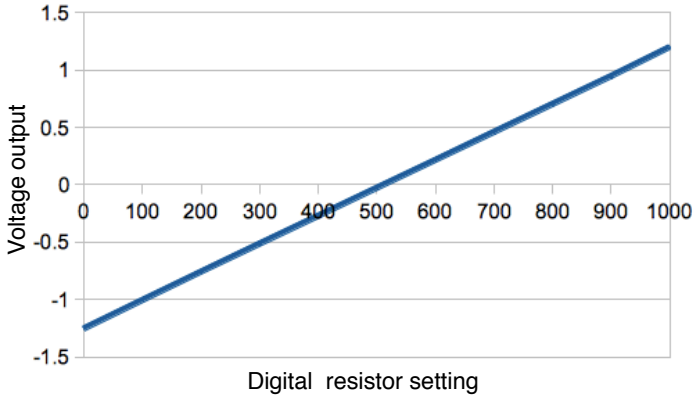


Figure 56: Measured threshold circuit output voltage as a function of digital resistor setting.

In the next step, the temperature sensors mounted on the front-end readout board were tested. To verify their correct operation, the front-end readout board was cooled to 15 °C and brought to the ambient temperature. The measurement of temperature as a function of time after the start-up of the board is shown in Fig. 57. The temperature reading was verified with a thermal imaging camera (Fig. 58). It was found that both sensors measured the same temperature within the error.

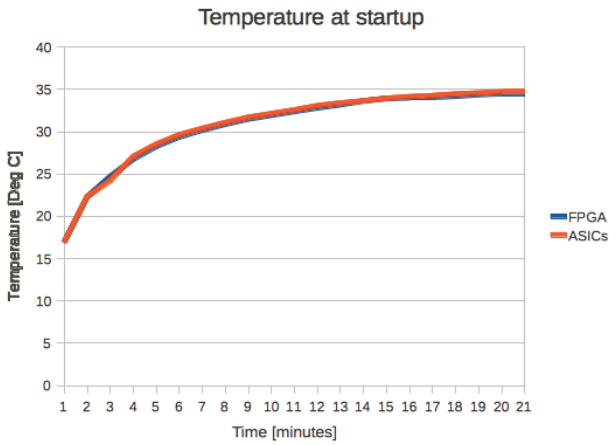


Figure 57: Temperature as a function of time after the board start-up.

Figure 58: The infra-red image of the ASICs side of the front-end board.

The next component of the board that was tested is a test pulse circuitry. During the tests, after the trigger, it automatically injects a controlled amount of charge into the input of the ASIC channels. By selecting the appropriate monitor signal, the board allows to monitor the internal signals of the ASIC on the oscilloscope. The response of the ASIC readout channel to the test pulse can be seen in Fig. 59.

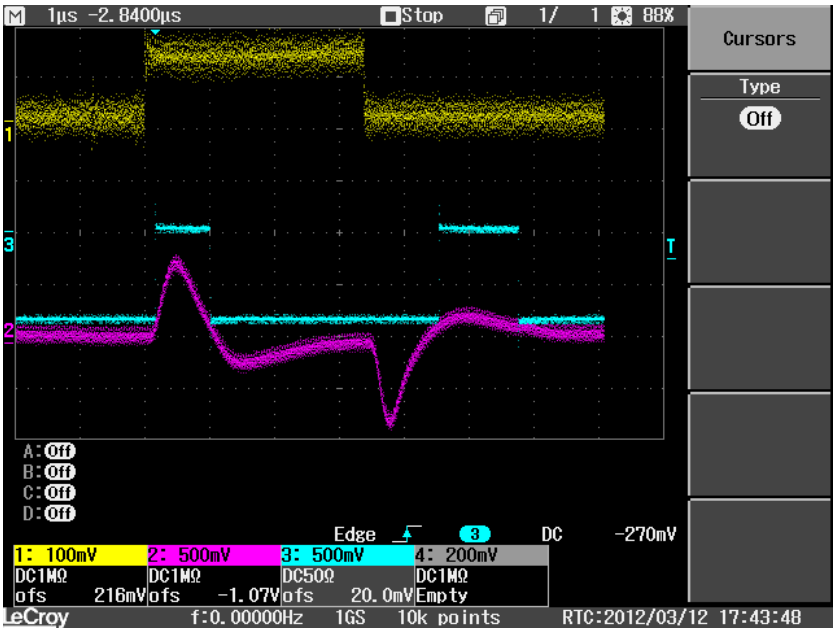


Figure 59: The response of the ASIC to the test pulse: injection signal (yellow line), ASIC analog response (violet line) and ASIC digital output (blue line).

By testing all this peripheral hardware components of the front-end readout board were can now move to the verification of the readout.

5.2 Functional verification of the readout system

As already explained in previous Section, the readout system allows three different readout modes. The run-time parameters that can be set are the shifting clock, the sending clock and the position parameter. The communication was verified by reading the fixed test data pattern (Fig. 60), equal on all the channels. I tested the communication for different sending clock settings and found that all the data were correctly transferred for different communication speeds including the 120 MHz sending clock which enables the final data transfer rate of more than 90 kHz, well above the Belle II requirements.

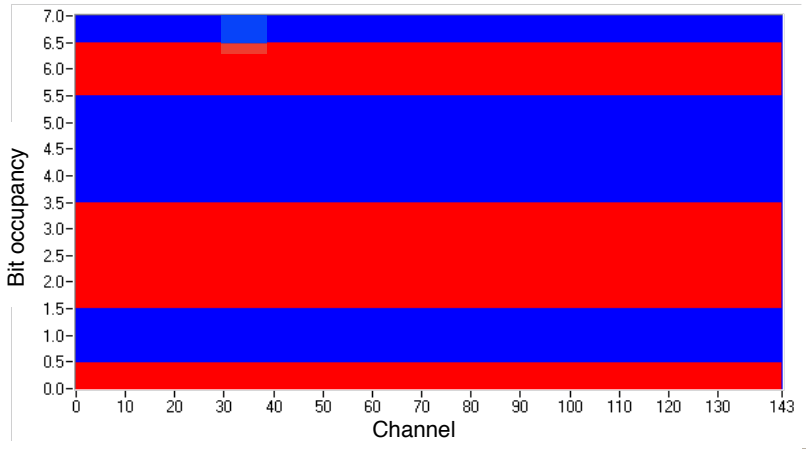


Figure 60: Test with a fixed data pattern: bit occupancy of 144 channels.

The initial tests of the detection algorithms were done without the HAPD sensor. The response of all channels to different values of the threshold voltage (threshold scan) was recorded. Even without any input signal, the ASIC chip has a baseline noise composed of frequencies around the shaping frequency.

In the edge detection mode, the measurement does not depend on the shifting frequency, in the following measurements 6 MHz shifting frequency was used. The threshold scan measurements without and with the test pulse were made. The test pulse with the height equal to the height of a single photon signal was used. The results of the measurements are shown Fig. 61.

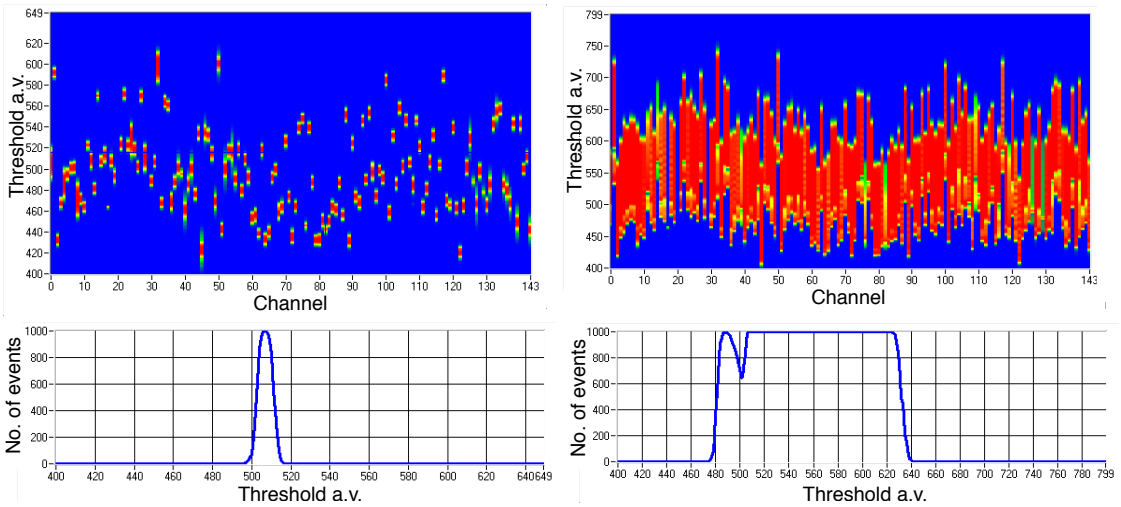


Figure 61: Threshold scan of a readout board in the edge detection mode without test signal - left and with the test signal - right. The response of all the channels (above) and for the channel 31 (bellow) to different threshold voltage settings for is shown.

The same measurements with and without the test pulse for the time over threshold mode of operation are shown in Fig. 62.

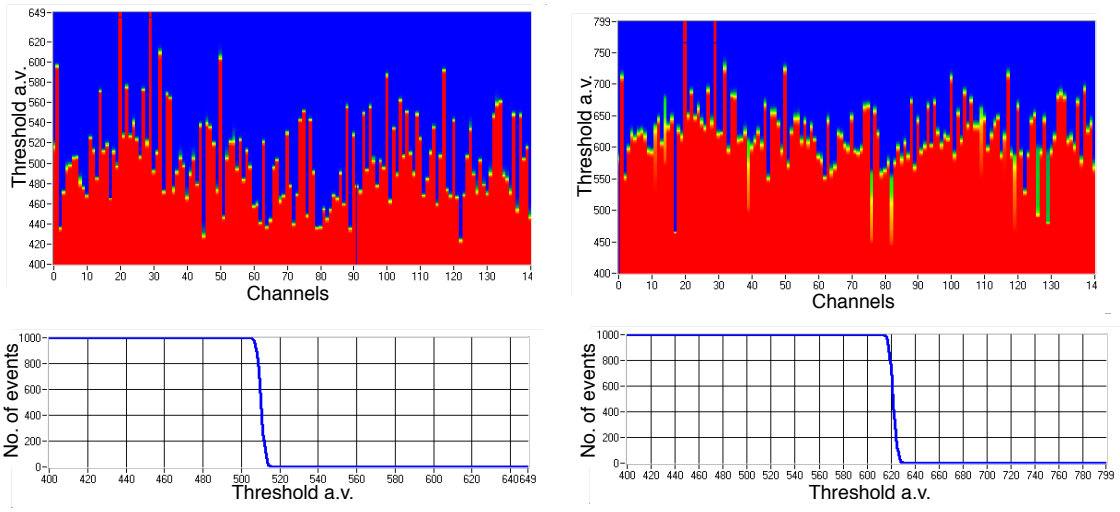


Figure 62: Threshold scan of a readout board in the time over threshold mode without test signal - left and with the test signal injected on all channels simultaneously - right. The response of all channels (above) and for the channel 31 (bellow) to different threshold voltage settings for is shown.

Due to different timings, the event data should be synchronized with the trigger. The position parameter sets the delay between the trigger and the

data (Fig. 63).

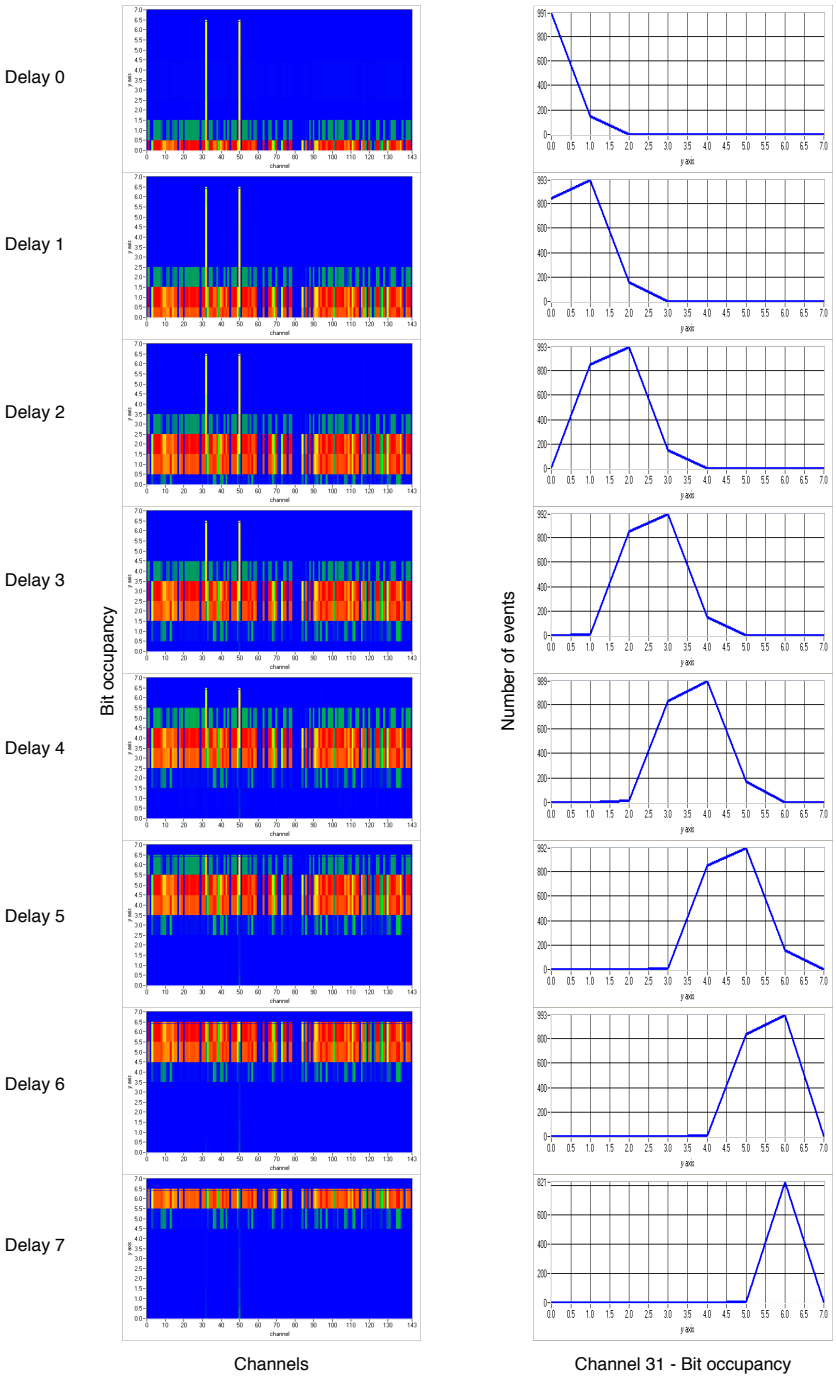


Figure 63: Synchronization of the data with the trigger: bit occupancy at different delay settings for all 144 channels (left), bit occupancy at different delay settings for channel 31 (right). Note how the peak of maximum occupancy moves with different delay settings.

The time over threshold mode requires match of the shifting frequency and the ASIC shaping frequency. At large shaping times the shift clock needs to be decreased. In Fig. 64 the bit occupancy is shown for different shifting frequencies for the case with the test pulse injecting the charge on all channels. The shaping time of the ASIC was constant during the measurements. The width of the distributions of the occupied bits is proportional to the time the HAPD signal was over the threshold.

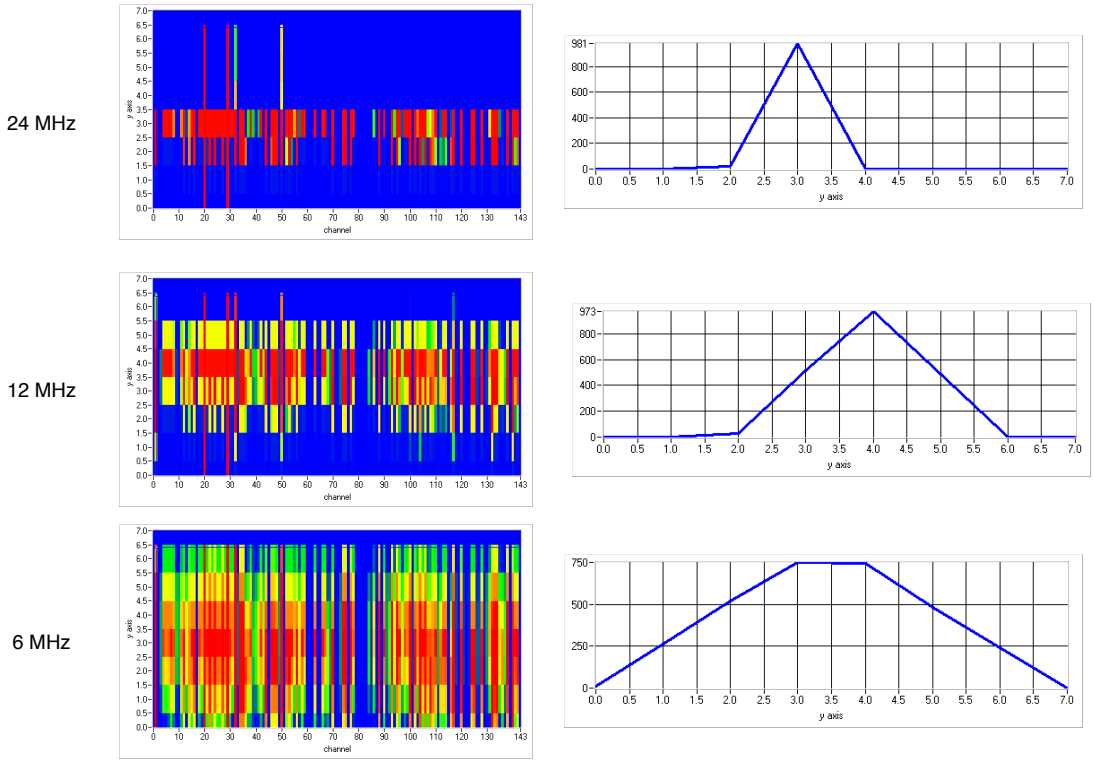


Figure 64: Time over threshold mode at different shift clock settings: bit occupancy for all the channels (left), bit occupancy of the channel 31.

An important parameter, which could degrade the performance of the aerogel RICH counter is the electronic cross-talk between channels. In order to evaluate the cross-talk of the ASIC chip (Fig. 65), test pulse signal was injected into a single electronic channel. By increasing the amount of charge, the response on the neighboring channel was measured. The effect was found negligible (Fig. 66).

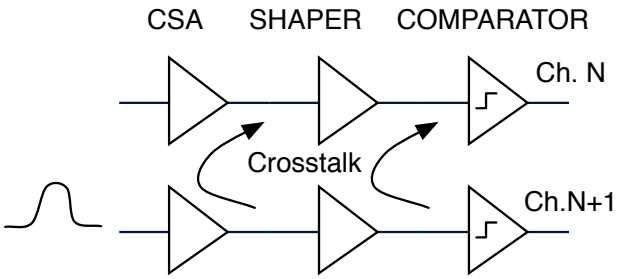


Figure 65: Schematic showing cross-talk between two neighboring channels.

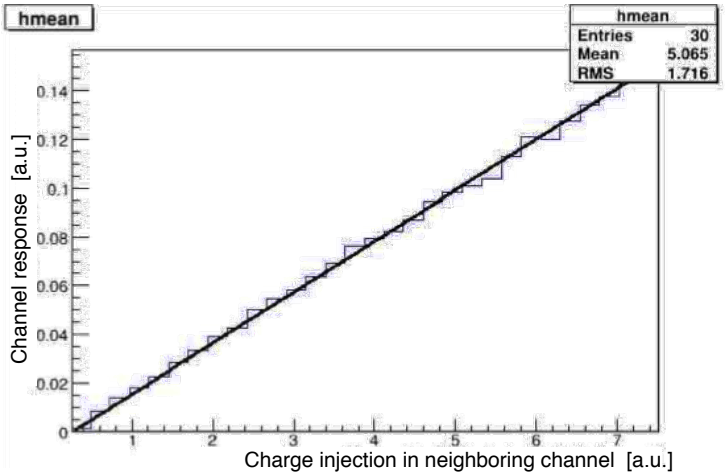


Figure 66: Cross-talk between two neighboring channels: channel response as a function of injected charge in neighboring channel.

5.3 Measurement with a triggered light source

Detection of single photons requires a light tight environment. A measurement setup was built inside a light tight box to evaluate the response of the HAPD and the readout board to short very low intensity illumination (Fig. 67). A blue light of 405 nm from a pulsed laser was guided into the light tight box via an optical fibre. In the box, one end of the fibre was mounted on a two dimensional translation stage with a step resolution of 100 μm controlled by a computer. The stage is used to position the light with respect to the HAPD sensitive area. The collimator in front of the fiber end and the small distance ($\approx$ mm) from the collimator to the detector resulted in the beam size width of 1 mm on the quartz window of the HAPD. The photon emission is a random process and the number of photons is distributed according to the Poisson distribution. The probability $p(n)$ that n photons is detected on the detector is:

$$p(n) = \frac{\bar{n}^n exp(-\bar{n})}{n!} \ . \tag{21}$$

It follows from the nature of the distribution that it is impossible to illuminate the detector with only single photons. One can however control the average number of photons by setting the power of the laser or by using filters. The laser also provided the output signal which was used to trigger the data acquisition. The electronic readout board was connected to the HAPD and attached to a non-movable frame and connected to the computer via CAEN V1485 IO board. In order to enable the single photon measurements, the readout board was first calibrated.

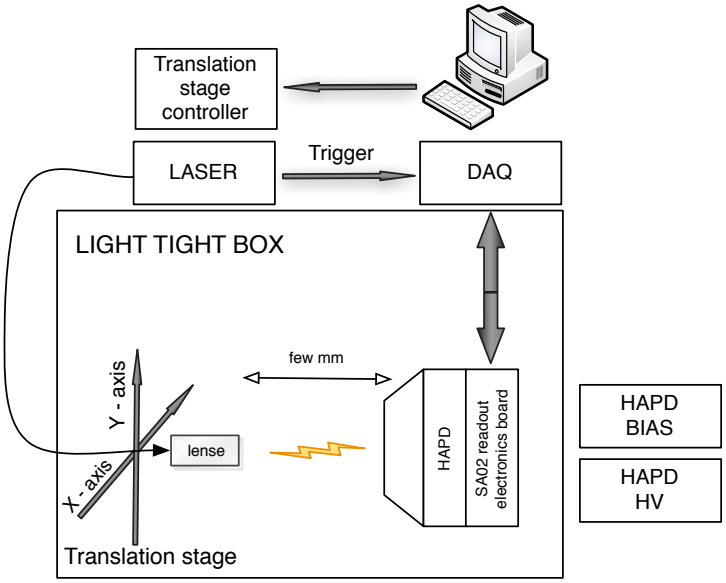


Figure 67: Setup of the apparatus for the measurement with triggered low intensity light source.

5.3.1 Calibration

After the connection of the HAPD to the readout board, the noise increased. This is attributed to the leaking currents and capacitance of the APD pixels. As a consequence the noise spread between channels varies and a calibration is required. Calibration of the board includes new configuration of channel offsets. To better explain the calibration procedure consider a threshold scan measured in edge detection mode (Fig. 68). The measured signal consists of noise from electronics and from HAPD, distributed normally with mean μ and dispersion σ.

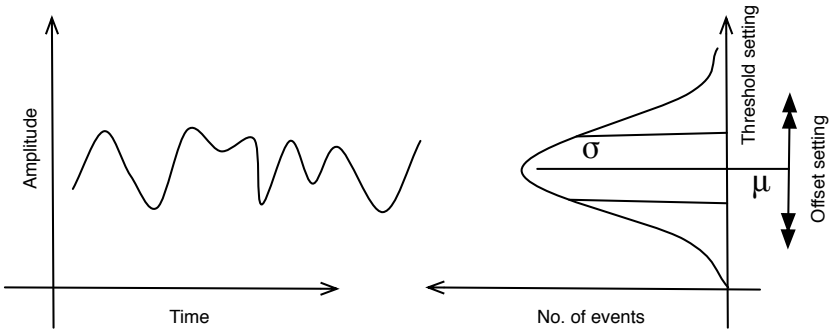


Figure 68: Threshold scan of a single channel without illumination.

The left side of the image shows a noisy signal with baseline in time domain. On the right side, the image shows a number of detected hits as a function of threshold setting. By changing the offset of the ASIC channel, the baseline position moves. The aim of the calibration is to align the channels with respect to a defined threshold value. The new offsets are calculated so that the distance of the channel mean μ to the set threshold is constant in terms of the signal spread σ. Typically a value of 3 to 5 σ is used. The σ and μ of each channel are obtained from a threshold scan in the edge detection mode. In order to make the calibration an initial set of parameters is loaded into the ASIC chip. The new offset parameters are calculated and written in the parameter file. By loading the file again the device is calibrated. Figs. 69 and 70 show the threshold scan for all channels for an uncalibrated and calibrated system using a time over threshold mode.

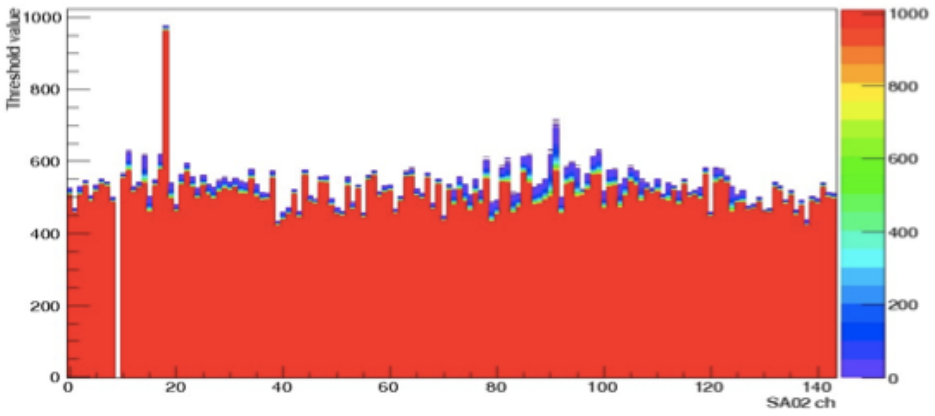


Figure 69: The threshold scan of the uncalibrated ASIC chip using the time over threshold mode. One of the channels is not working correctly.

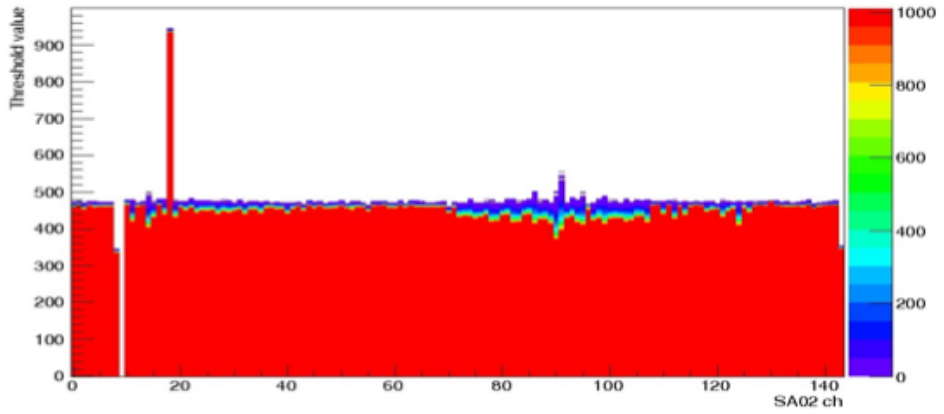


Figure 70: The threshold scan of the calibrated ASIC chip using the time over threshold mode. One of the channels is not working correctly.

The same measurement was done in the edge detection mode. Figs. 71 and 72 show the response of all channels as a function of the threshold voltage for uncalibrated and for calibrated system.

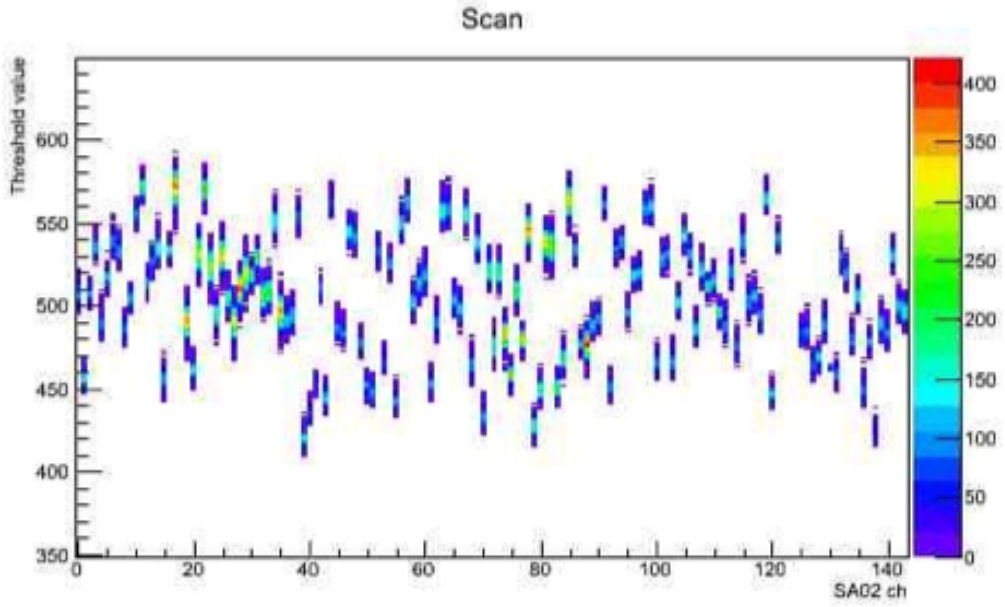


Figure 71: The threshold scan of uncalibrated ASIC chip scan using edge detection principle.

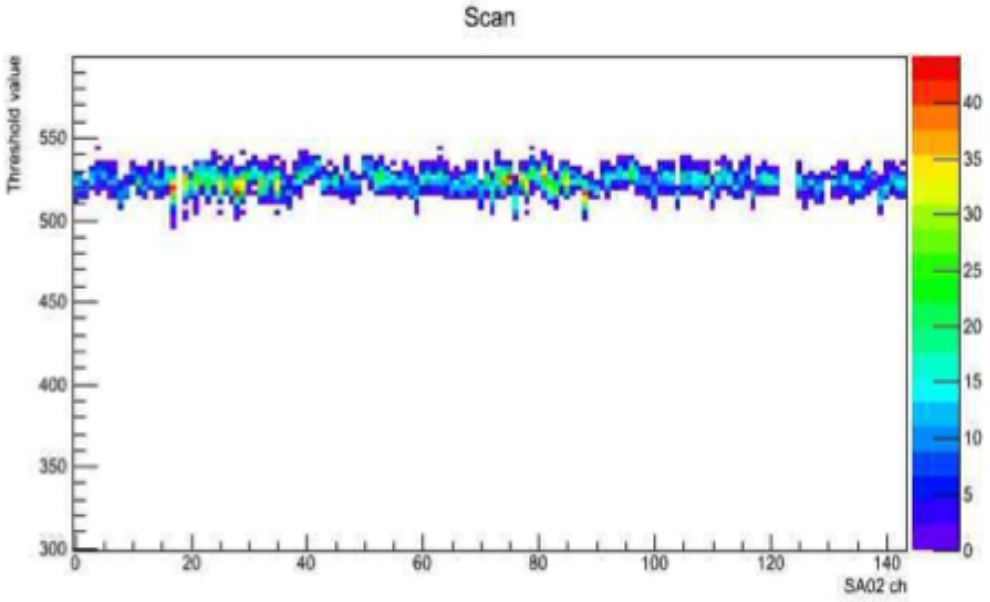


Figure 72: The threshold scan of calibrated ASIC chip using edge detection principle.

5.4 Results

The response of the HAPD to several photons is measured in both modes: edge detection and time over threshold. Fig. 73 shows a threshold scan for a single channel illuminated using the edge detection principle. The photon peaks in the scan appear clearly separated from the noise pedestal. A similar result shown in Fig. 74 is obtained by measuring a threshold scan using the time over threshold measurement principle.

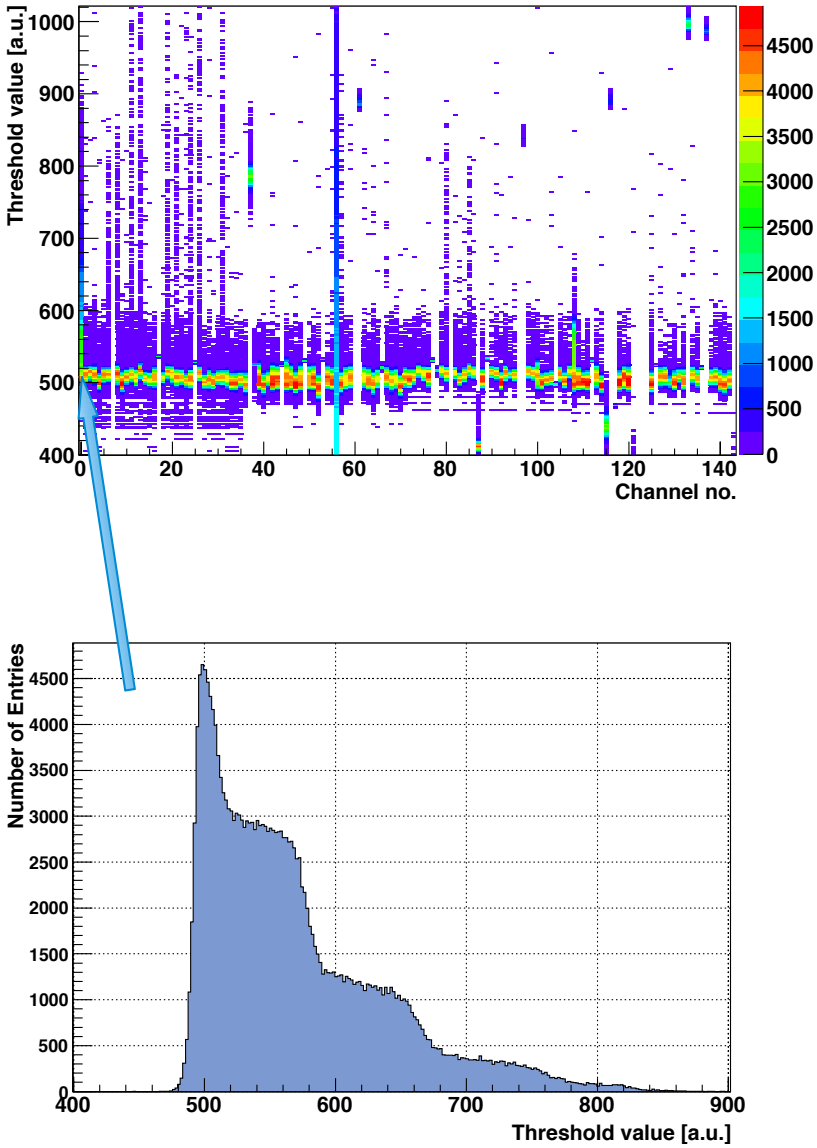


Figure 73: Response of all channels (top) and single channel (bottom) of the HAPD to a single channel illumination as a function of the threshold voltage for edge detection mode.

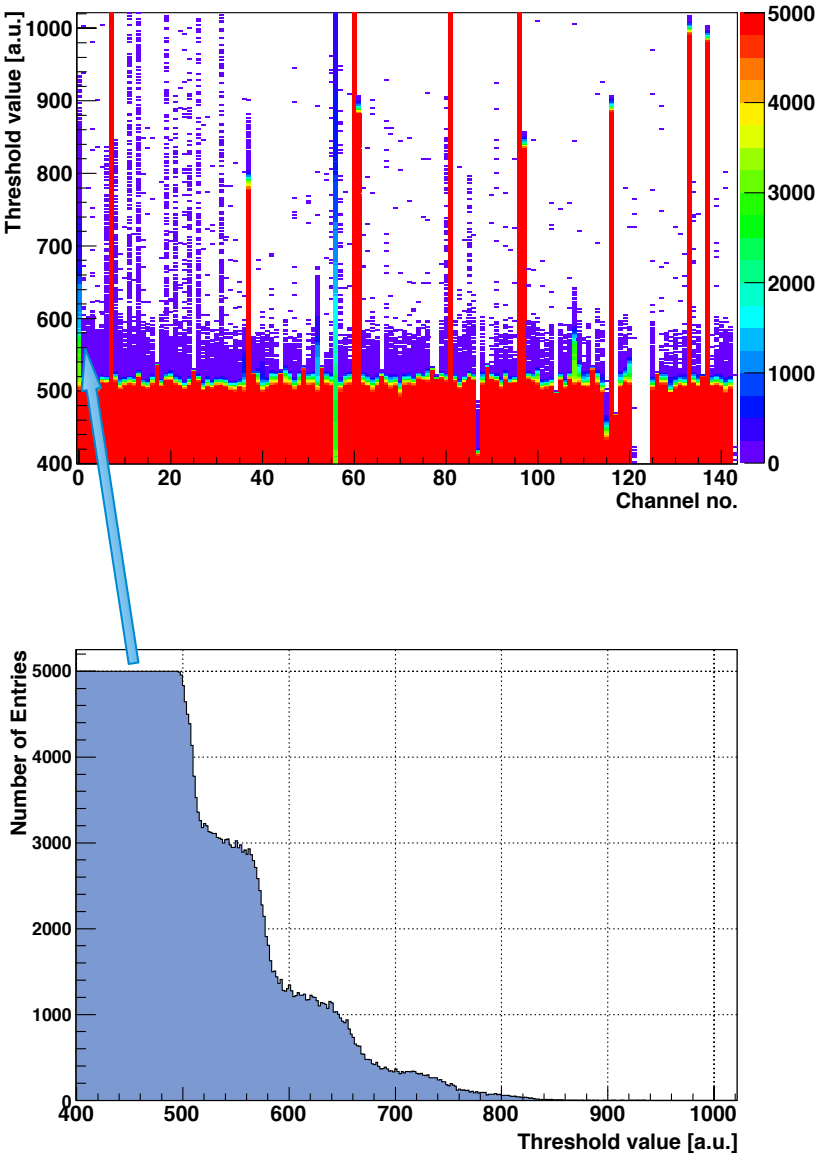


Figure 74: Response of all channels (top) and single channel (bottom) of the HAPD to a single channel illumination as a function of the threshold voltage for time over threshold mode.

The time over threshold mode, apart from enabling hit detection aims as well to provide an estimation of the time of the signal being above the threshold level. A triangular shaped signal such as that from the SA02 ASIC shaper circuit, starts increasing its width when the amplifier slowly rolls out of its linearity and begins saturating. At a gain setting of 60 mV/pC this happens at a signal of height of about 3 photons.

Consider the case of illuminating a single channel with mostly single

photons for acquiring data. Subsequent measurements of data bit occupancy at different threshold settings are shown in Fig. 75.

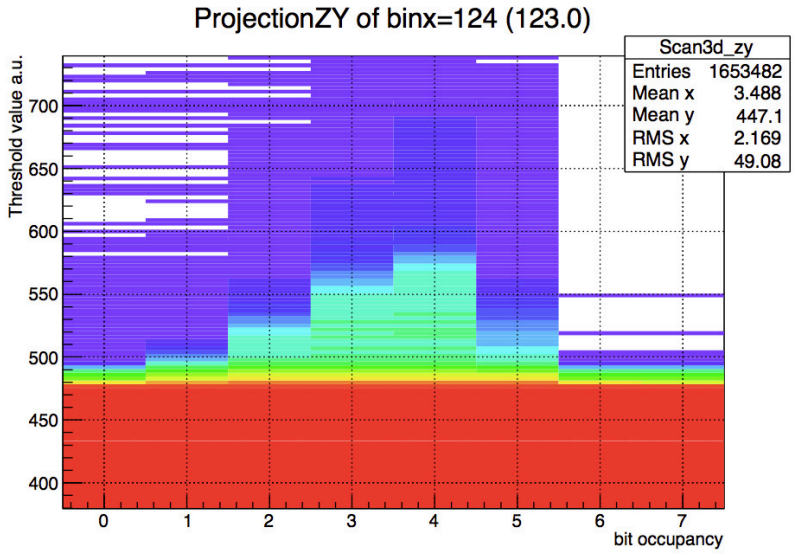


Figure 75: Bit occupancy as a function of a threshold voltage for a channel illuminated with several photons with readout board in the time over threshold mode.

The structure in the image is a reconstruction of the original analog signal from the shaper. The color represents an indication of the number of events which follows the ratio from the threshold scan. The traces from single, double and triple photons can be quite clearly seen.

The readout in both detection modes works as expected and the detection efficiencies for the different measurement principles can be compared. For a single channel illumination with mostly single photons the response of the readout in two detection modes is plotted in the Fig. 76.

It is good practice to compare response of a system with the response in some other measurement unit to crosscheck the operation. We wanted to ensure that the detection efficiency is comparable with another independent equipment. The CAEN V729 is an 4 channel ADC VME module which can record wave-forms similarly to an oscilloscope with a 12 bit resolution at a sampling frequency of 40 MS/s [29]. In order to measure the response, the analog signal from the shaper circuit was amplified to adapt the signal pulse height to the input of the ADC module input that ranges from 0 to 2 V. The accumulated wave-forms recorded by the CAEN V729 can be seen Fig. 77.

From the waveform the charge can be extracted by integrating the positive value of the waveform (Fig. 78).

The measurement obtained with the ADC module shows a clear separation of the noise pedestal from single, double and multiple photons. In order

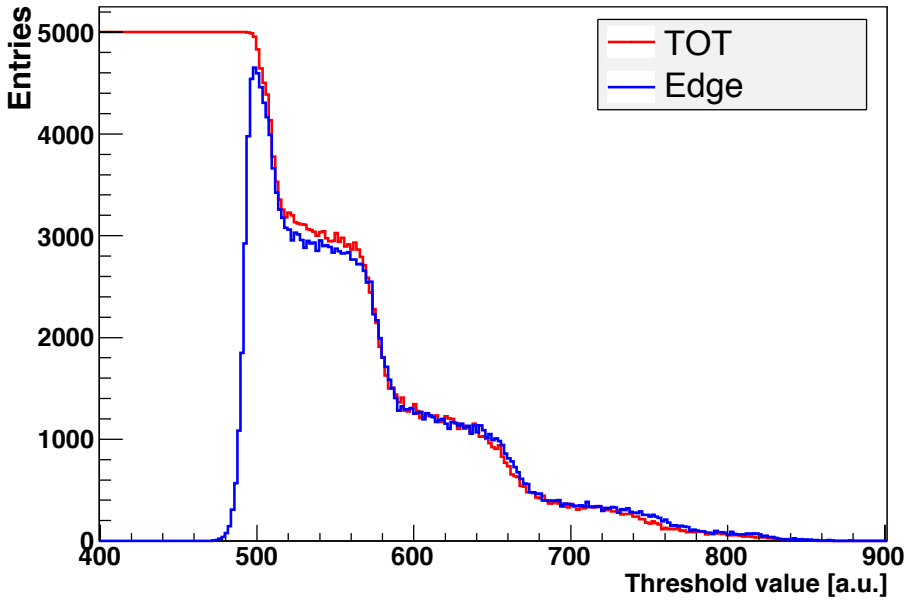


Figure 76: Comparison of the two detection methods. No. of detected events as a function of threshold value for edge and time over threshold mode.

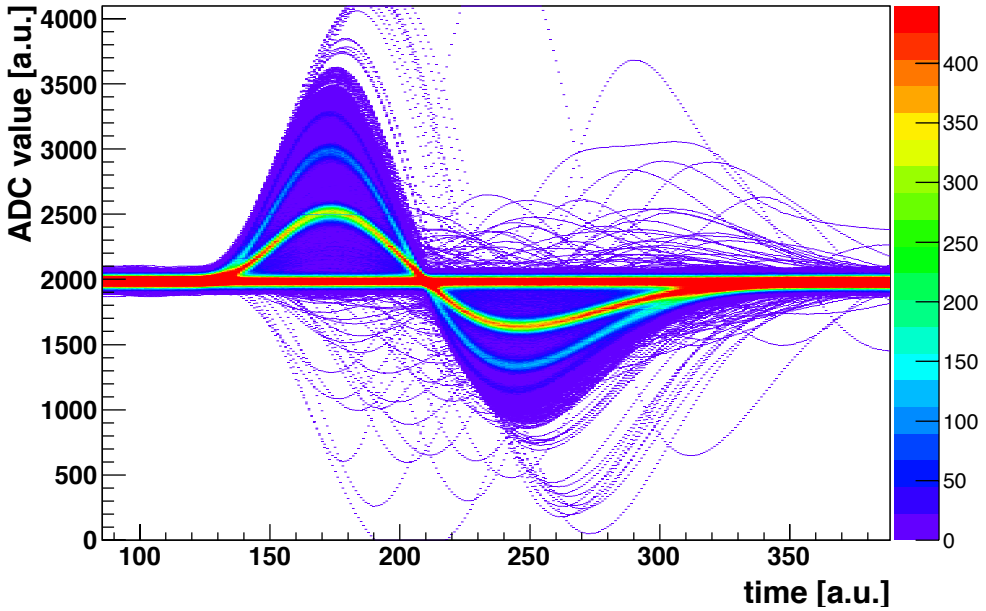


Figure 77: Accumulated signal waveform measured with ADC CAEN V729. Single channel amplitude response as a function of time.

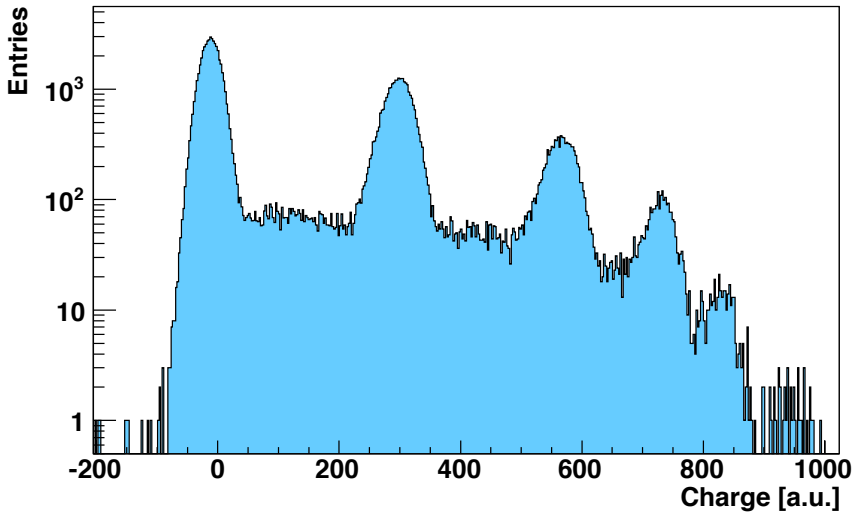


Figure 78: Charge distribution extracted from the waveform measurements with CAEN V729 module.

to compare the results of the ADC with the DAQ threshold scan, the easiest way is to transform the ADC charge distribution into a threshold scan. By integrating the charge distribution, the response similar to the threshold scan with the readout board can be obtained (Fig. 79).

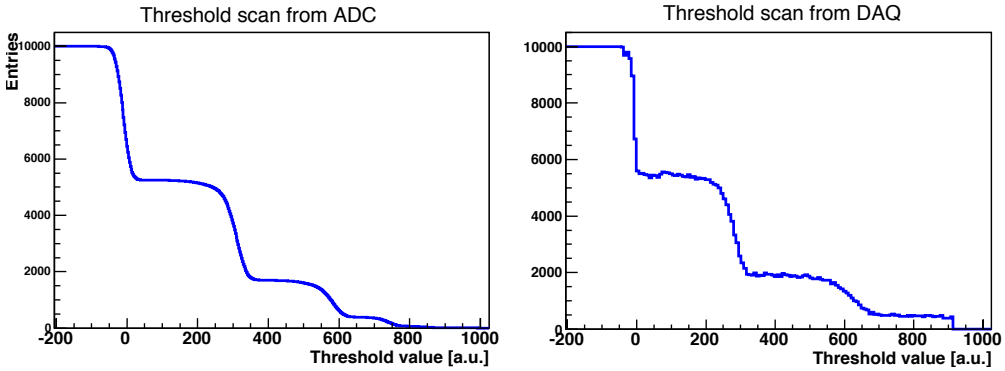


Figure 79: Response of the HAPD as a function of the threshold value: integrated charge distribution from CAEN V729 (left) and measurement with the readout board.

By using the readout, a two dimensional scan with the light across the surface of the sensors active area was performed. The HAPD channel with the highest event number is recorded. The outcome picture of the HAPD pixels is clearly visible in Fig. 80.

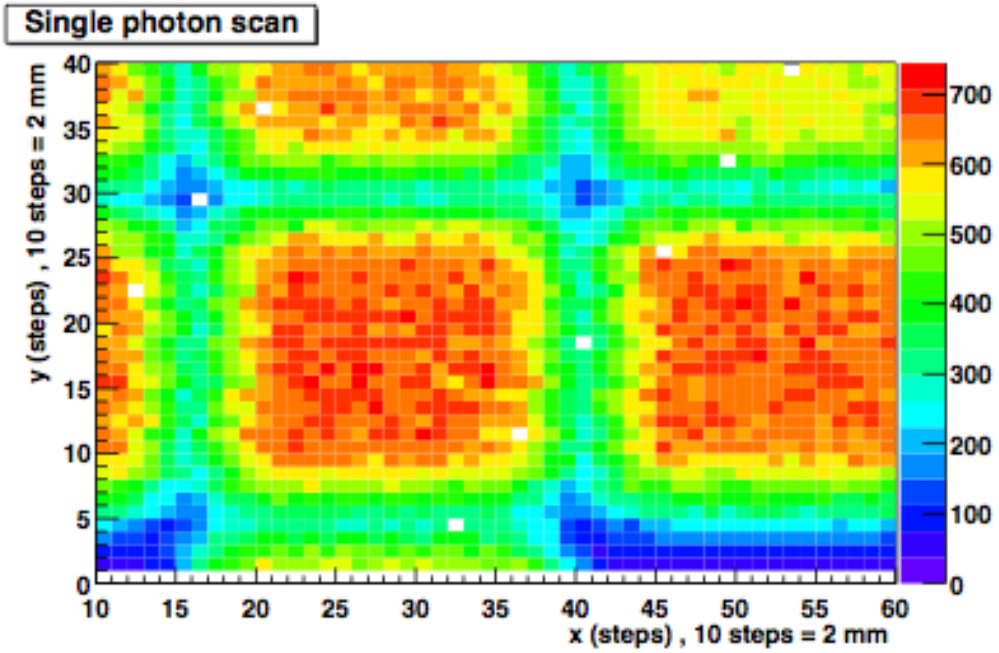


Figure 80: Partial HAPD 2D scan with mostly single photons.

The histogram shows a good uniformity of the APD pixel active area and the separation between pixels.

5.5 Analysis of time over threshold principle for particle track detection

Charged particles moving through the aerogel RICH detector emit Cherenkov photons in the quartz windows of the photon sensors as well. To improve the separation capabilities it would be good if photons originating from quartz window can be separated from photons emitted from the aerogel.

The quartz entrance window (Fig 81) has a refractive index of approximately 1.5 and acts as Cherenkov radiator and emits about 100 of Cherenkov photons.

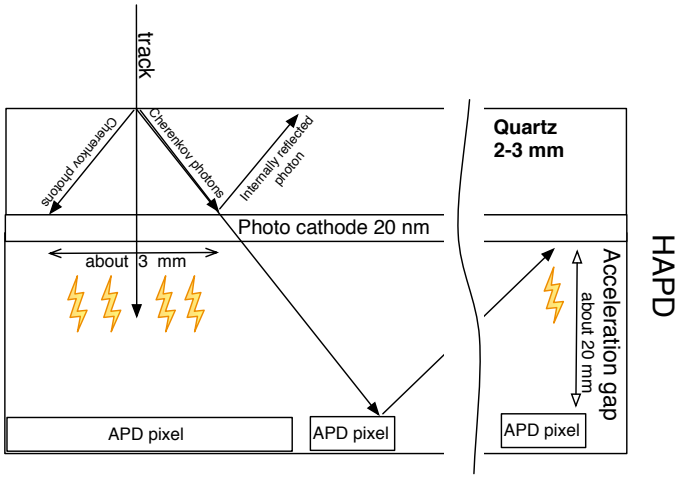


Figure 81: Production of Cherenkov photons in quartz window of the HAPD. Most of the photons originating from the quartz window produce photoelectrons in the photo cathode. Some photons pass the photo cathode and reflect on the surface of the APD pixels emitting photons when exiting the HAPD through the quartz window. A small portion of photons is internally reflected in the quartz window.

Basf2 [30] is a software framework based on Geant4 [31] and contains the structure of the aerogel RICH detector. This allow to simulate the response of the aerogel RICH detector. The simulation accounts the aerogel radiator, photo cathode quantum efficiency and HAPD geometry. A simulation of 10000 events was made to verify the quantity of photons produced by tracks. Fig 82 shows one event photon distribution.

An estimate is that 18 photo electrons will be created within the track passage through the quartz window. The area covered by photo electrons is about 7 mm^2. This is below the APD pixel area and most likely the charge will fall on a single APD pixel.

The pulse length of the signal could be extracted within certain accuracy with time over threshold mode of measurements.

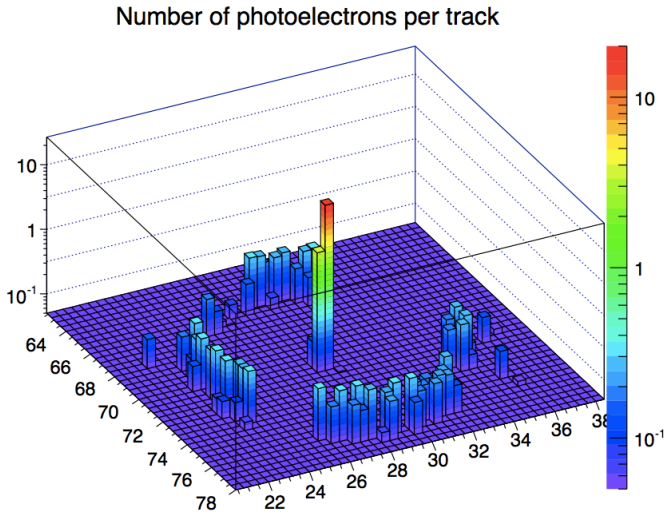


Figure 82: Simulation of an event in the aerogel RICH detector.

The test pulse system was used to verify the response of the ASIC chip in the presence of larger signals. Charge was injected into a single channel and the pulse length with time over threshold was measured. Fig. 83 shows the result of subsequent measurements of data bit occupancy as a function of injected charge in photon peak equivalent level. The shifting frequency corresponds to 166 ns per cycle. The data bit occupancy is directly related to the measurement of the time of the signal above the preset threshold.

Using the same algorithm but varying the shifting frequency to 250 ns per cycle, a larger signal can be recorded (Fig. 84). The presented result shows a charge injection equivalent up to a level of 16 photons. The spread of the occupied bits is less evident since the clock rate is slower and the effect of the not completely synchronized charge injection in regard to the internal shifting frequency makes it less evident. The amplifier clearly enters into saturation at about 3 photon level peak reaching a plateau. By even increasing the amount of charge on the input of the ASIC, the time over threshold signal extends additionally.

The time over threshold can be used as a discrimination parameter to reject hits which are above the certain value and can provide an additional information in the particle identification algorithms.

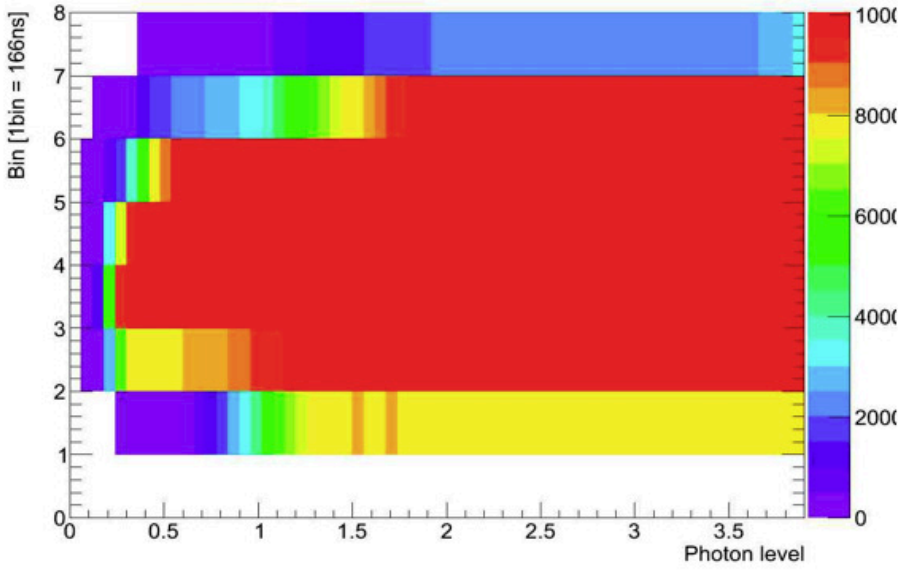


Figure 83: Bit firing probability vs. injected charge in photon level units - buffer length 1.3 μs.

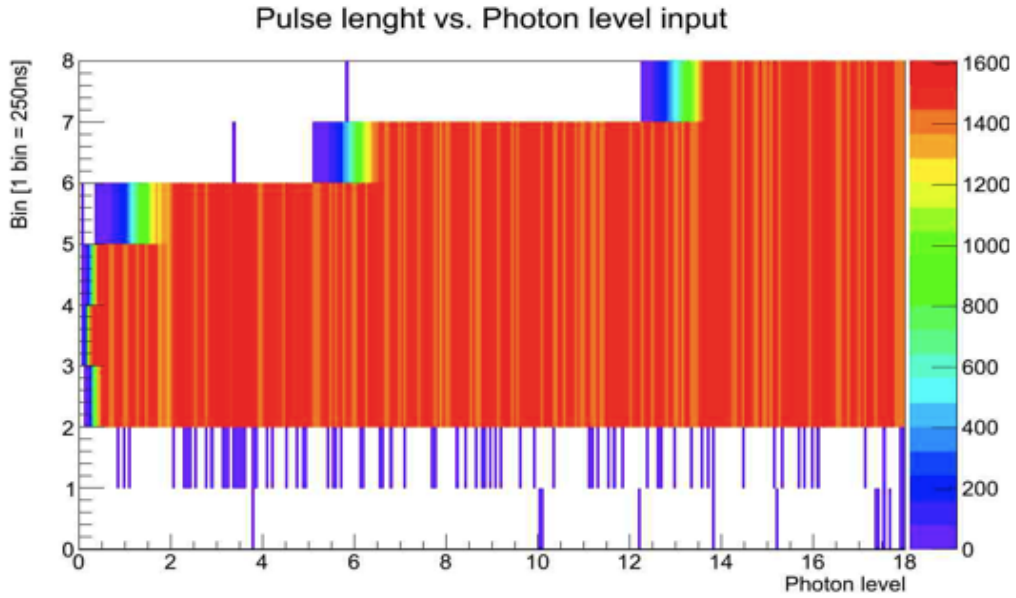


Figure 84: Bit firing probability vs. photon level - buffer length 2 μs.

6 Operation in magnet and during irradiation

The HAPD sensor and the readout board should operate in a magnetic field of 1.5 T and in the presence of radiation during the 10 years life time of the experiment. The readout board does not use any component made of ferromagnetic material and we did not expect problems with its operation in magnetic field. The major vulnerability is the exposure to radiation: a flux of 13×10^{10}neutrons/cm^{2}year of 1 MeV equivalent neutrons is expected in the area of the aerogel RICH detector, while the total gamma irradiation is estimated to around 100 Gy per year [9]. The HAPD sensor has been designed and tested to withstand such a radiation.

The electronic front end board houses ASIC chips, FPGA and other peripheral components. The ASIC chip (SA03 version) was designed with double registers for settings and is expected to withstand the expected irradiation. Up until now, the FPGA and support circuitry has not yet been tested.

In the next two subsections I will analyze the operation of the readout system in the presence of a magnetic field and in radiation environment.

6.1 Test in magnetic field

At the KEK institute in Tsukuba, Japan, the research group operates an 80 kW electro magnet. The magnet is composed of a large two C shape laminated iron core winded with copper tubes. Cooling of the device is provided with cold water flow through the tubes. The magnet (Fig. 85) has an active volume 0.5 m $\times$ 0.5 m $\times$ 0.3 m wherein the magnetic field is homogeneous to a first approximation. The measurement setup was mounted in a light tight box which is mounted on rails to simplify the insertion of the setup into the magnet.

Inside the box, a two dimensional translation stage is used to scan the active surface with a light beam brought into the light tight box via an optical fibre from a laser (Fig. 86). The direction of the magnetic field is perpendicular to the HAPD active surface. The focusing lens is positioned a few mm above the quartz entrance window of the HAPD and focuses the light beam into a spot with area of about a mm^2.

The measurement system is composed of:

- HAPD with electronic readout board
- Laser of wavelength of 400 nm
- Translation stage
- Ortec fast amplifier

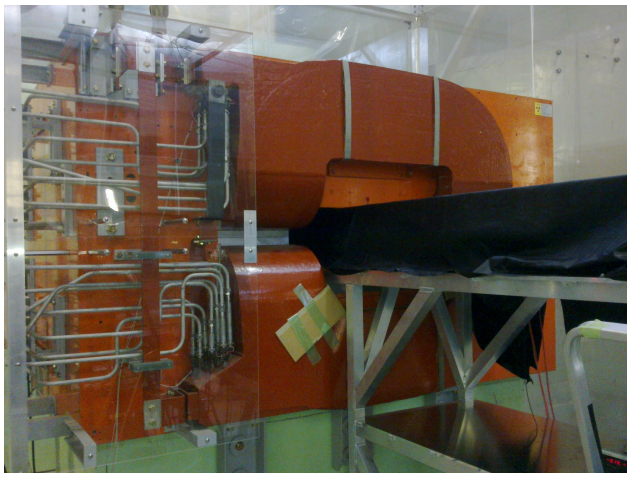


Figure 85: The 80 kW magnet with 1.5 T homogeneous magnetic field.

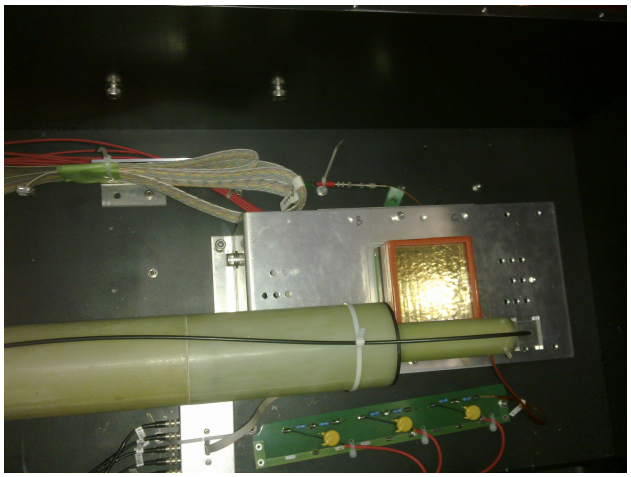


Figure 86: Light source positioning system and the HAPD fixed in the frame.

- VME system
- VME readout system
- VME ADC V729
- Oscilloscope

The measurement setup uses an HAPD coupled with a front end board and the DAQ readout system. The ADC system, the CAEN V729 ADC, was used to compare the results. A computer program positions the light beam over the HAPD sensor and acquires data. The trigger is provided by the laser which activates the measurement. The setup is shown in Fig. 87.

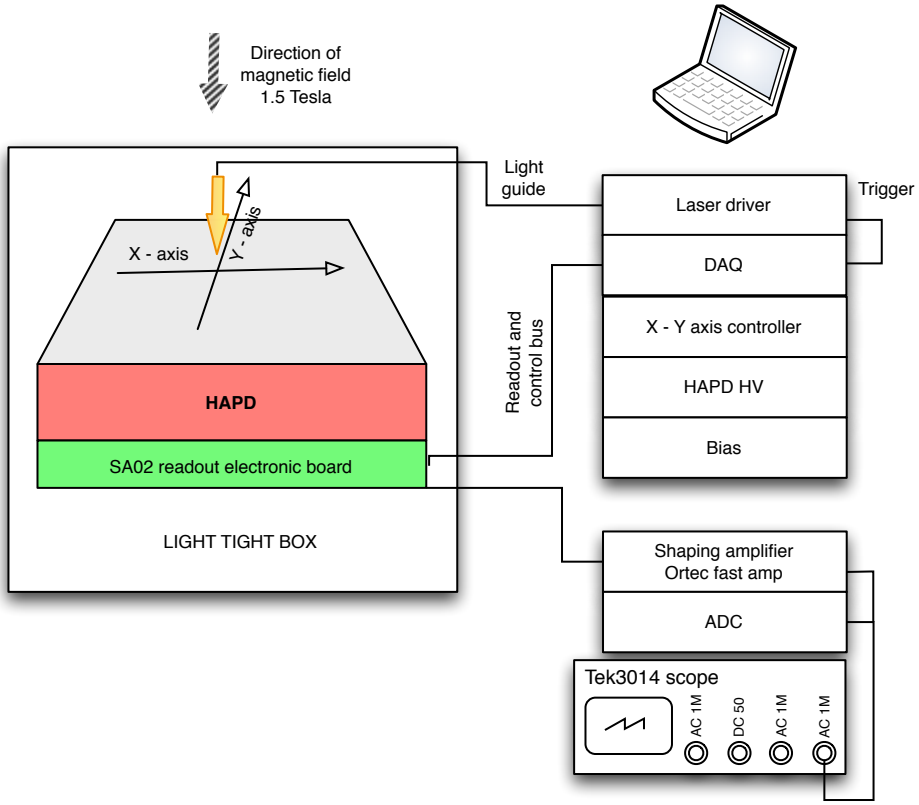


Figure 87: Schematic of the measurements setup for measurements magnetic field.

6.1.1 Measurements of illuminated channels using an ADC

Two measurements were done with and without the presence of the 1.5 T magnetic field with the ASIC shaper output. The data were acquired with an oscilloscope and with the ADC module. The oscilloscope images are shown in Figs. 88 and 89.

The measurement with the ADC resulted in the charge distribution with and without magnetic field shown in Fig. 90. The first peak corresponds to the noise. The following peaks are due to single, double and triple photon hits. Note that in presence of the magnetic field the peaks slightly increase. This effect was already noticed during previous measurements [32]. In presence of magnetic field, the trajectory of the electron traveling inside the HAPD is coiled around the magnetic field lines. As a consequence, the effect of electron back-scattering from the APD surface is reduced. The electrons will, in presence of the magnetic filed, land very near on the APD surface to the location where the primary photo electron was created. Contrary the back-scattered electrons land typically in a radius of about few mm from

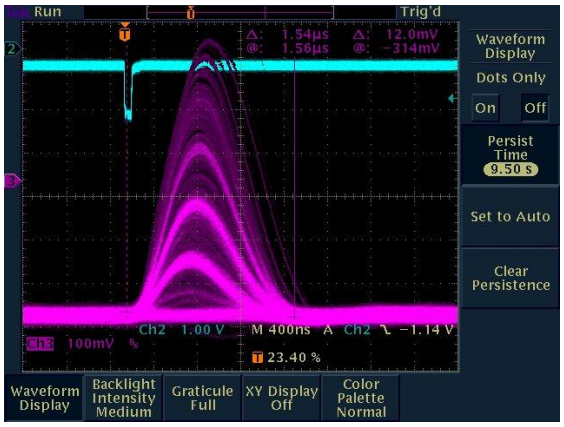


Figure 88: ASIC response to mainly single photons at B=0 T.

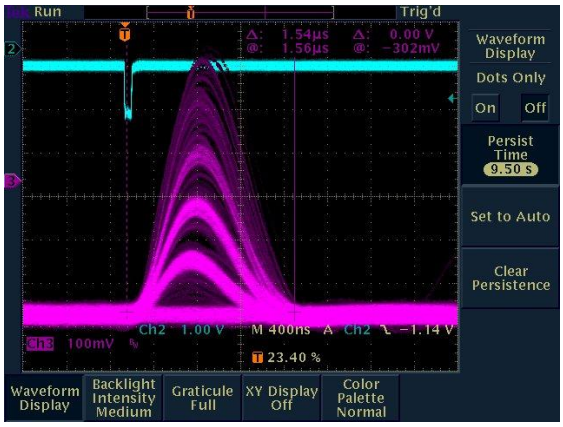


Figure 89: Response to mainly single photons at B=1.5 T.

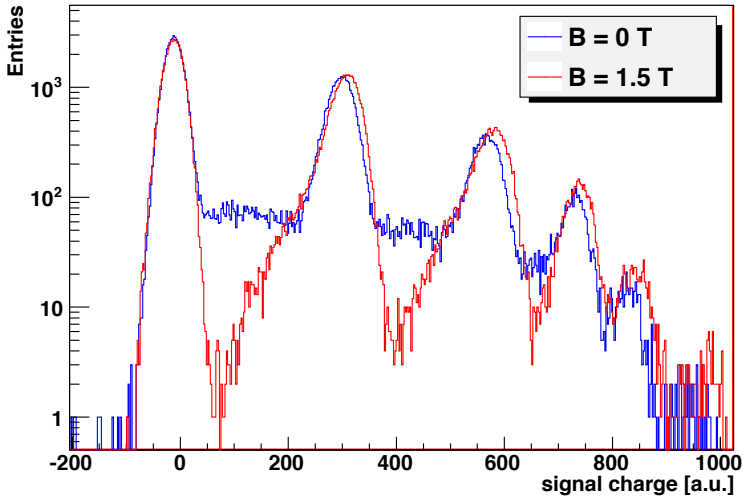


Figure 90: Single channel response, accumulated charge distribution, measured with ADC.

the initial position. This makes the difference in collected charge spread and reflects in worse operation.

6.1.2 Measurement in magnetic field with the front end board

The next step was the test of the front end electronics. For the cases with and without the magnetic field the single channel was illuminated and the data collected for both modes of operation: edge detection mode and time over threshold mode. The results shown in Figs. 91 and 92 show the expected increase of performance in the presence of magnetic field. We can conclude

that the readout board is operational in magnetic field of 1.5 T and it can be used as a front end board in the aerogel RICH detector of Belle II.

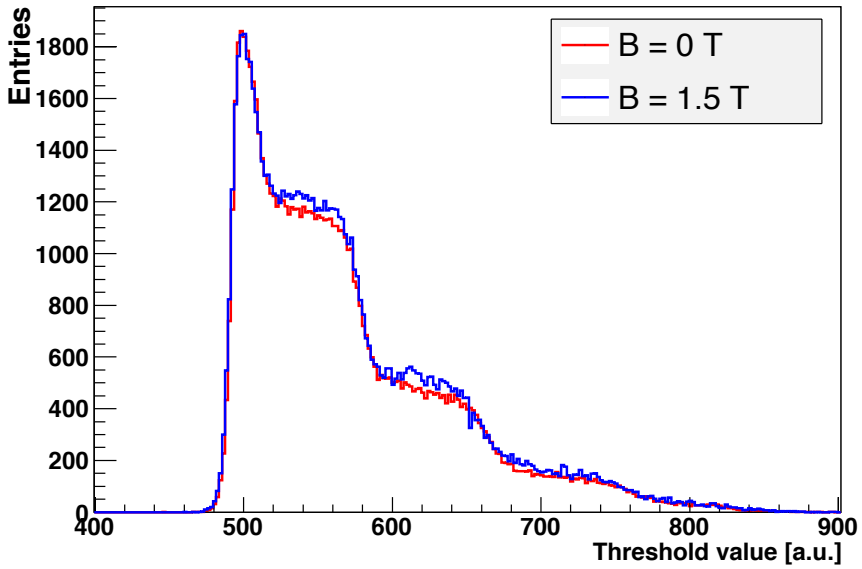


Figure 91: Threshold scan measurement of an illuminated channel using the readout board in edge detection mode with and without magnetic field: number of detected events as a function of threshold value.

6.1.3 Surface sensitivity of the HAPD in the magnetic field.

To test the surface sensitivity of the HAPD connected to the readout board, first the gain variation in the centers of HAPD pixels was measured by measuring the response of the sensor to the light beam in the channel center as a function of the threshold voltage (Fig. 93). The results show a uniform gain response for all channels.

In the next series of measurement, the surface of the HAPD was scanned with the light beam. The threshold was fixed to a level to detect single photons. For each pixel row a linear scan over the pixel centers was performed. In the case without magnetic field (Fig. 94) one can clearly see the distortions due to the non homogeneity of the electric field at the edges of HAPD enclosure which displaces the electron trajectory. In the presence of magnetic field, this effect is compensated and the incident photon position can be determined from the hit channel (Fig. 95).

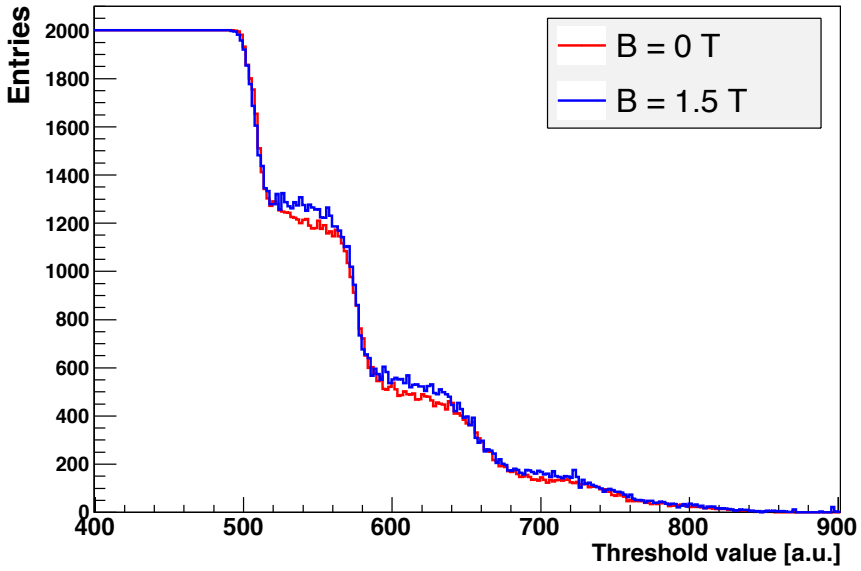


Figure 92: Threshold scan measurement of an illuminated channel using the readout board in time over threshold mode with and without magnetic field: number of detected events as a function of threshold value.

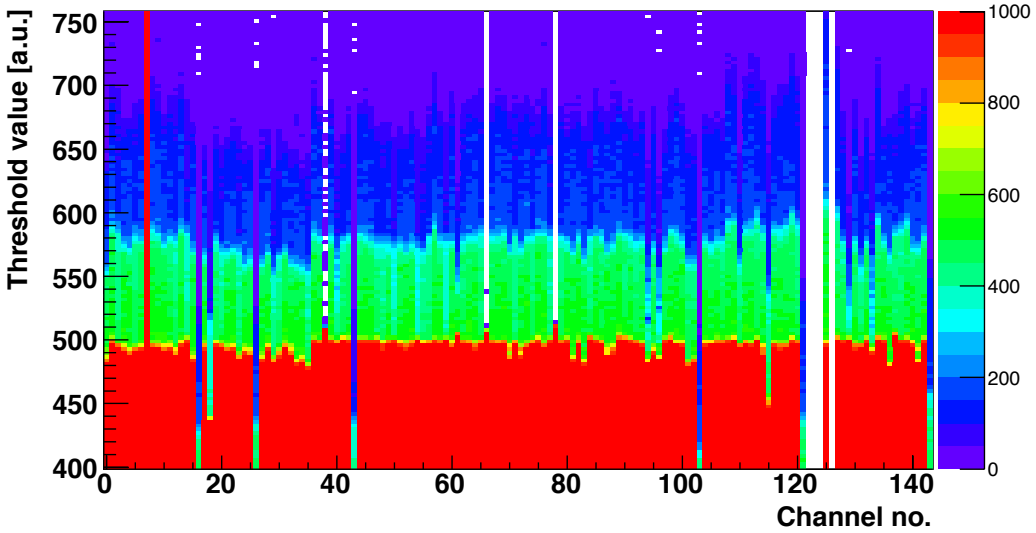


Figure 93: 2D scan / Threshold scan, response to mostly single photons for 144 channels.

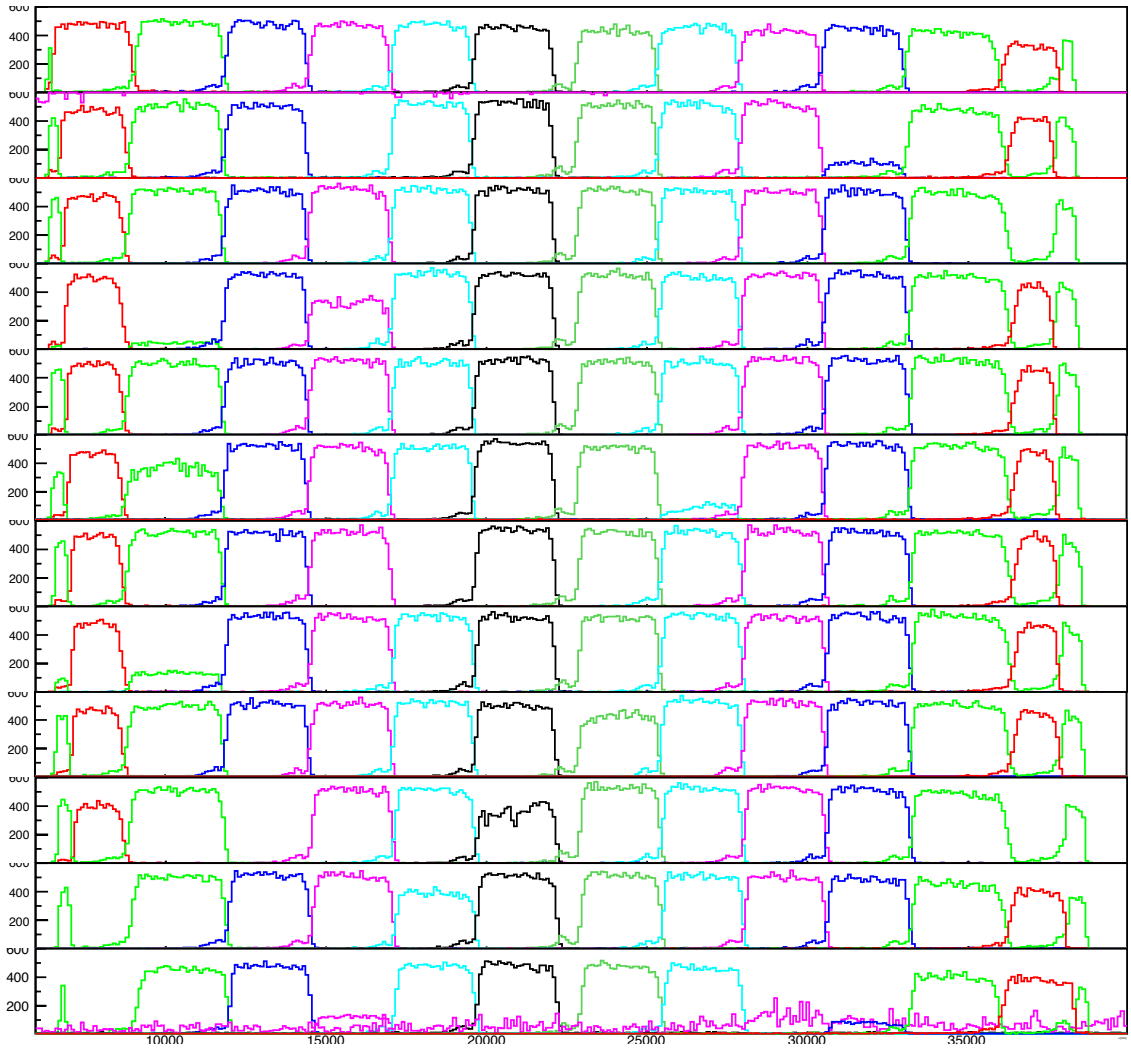


Figure 94: Surface sensitivity of the HAPD without magnetic field. Response to a focused laser light of low intensity (mostly single photons). Each row corresponds to a scan over the centers of the HAPD pixels of one HAPD row.

6.2 Test in radiation environment

In the Belle II environment the elevated radiation levels are expected to reach $\approx 10^{12}\,\mathrm{n/cm^2}$ in ten years of operation (Fig. 96). The expected levels have been obtained by using Geant4 [31] based Belle II software framework Basf2 [30], where almost all detector components are properly described and their response to different types of background contributions simulated. In a series of tests we tested the photon sensors during and after neutron and gamma irradiation. After these tests we selected the type of HAPD which is most radiation resistant, i.e. shows the least increase in the leakage current and has the highest signal to noise ratio [33].

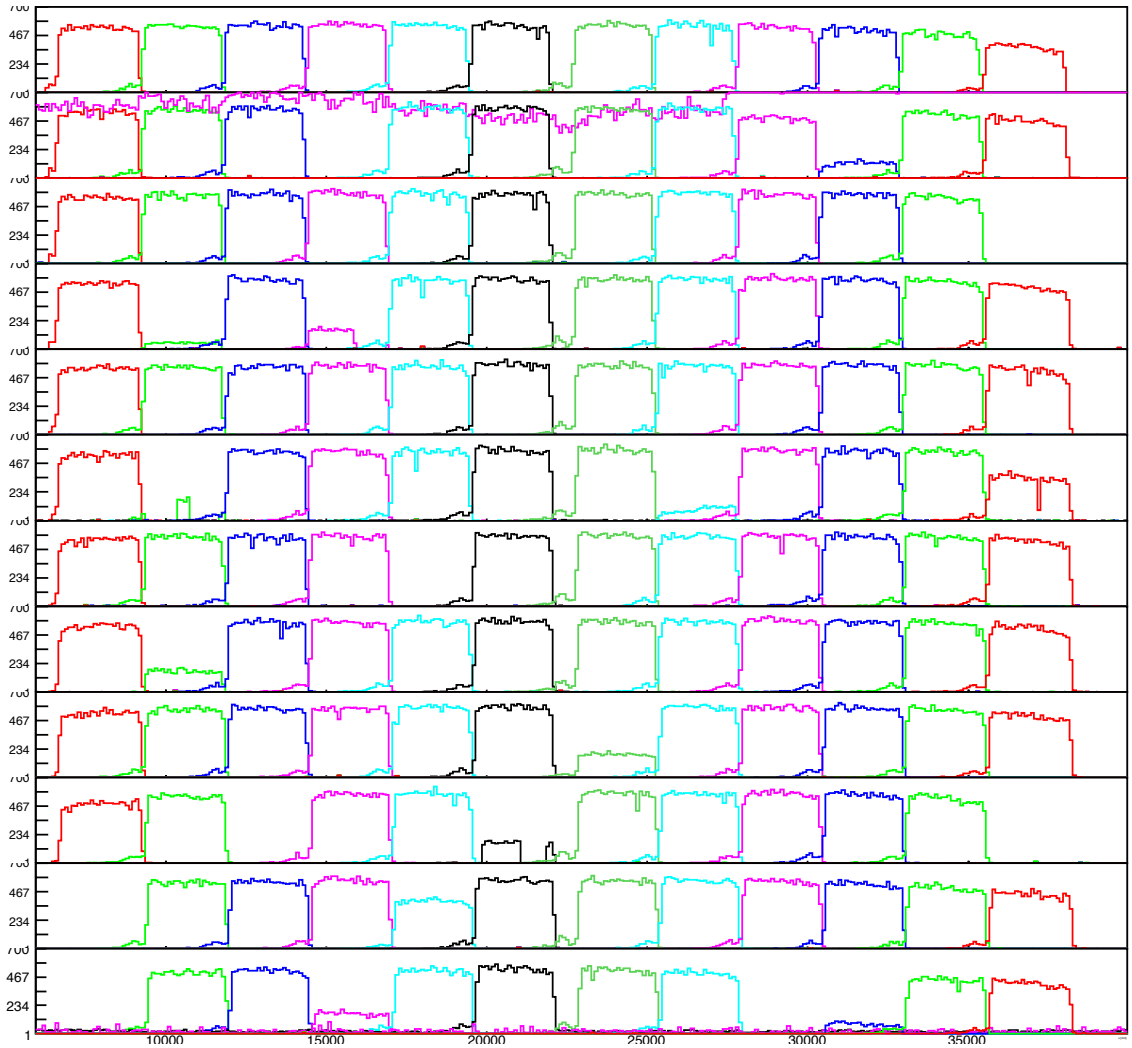


Figure 95: Surface sensitivity of the HAPD in the magnetic field of 1.5 T. Response to a focused laser light of low intensity (mostly single photons). Each row corresponds to a scan over the centers of the HAPD pixels of one HAPD row.

To test the readout electronics in the environment similar to the one in the Belle II detector, we have performed several tests [34] in the TRIGA Mark II reactor at the Jožef Stefan Institute, Ljubljana [35]. TRIGA is a 250 kW light-water reactor with an annular graphite reflector cooled by natural convection. It has several irradiation channels in the core. The most useful for the measurements of the detector modules are the triangular irradiation channel in the reactor core with flux of 1 MeV equivalent neutrons of 10^{12} n/cm^2/s and a dry chamber at the side of the reactor core with flux of 1 MeV equivalent neutrons of 10^7 n/cm^2/s (Fig. 97).

One of the possible limiting factor in the use of the readout electronics

in Belle II is the use of Spartan-6 FPGA. In Spartan-6 boron is used as a p-type dopant in production of silicon wafers because it diffuses at a rate that makes junction depths easily controllable [36]. Unlike in other FPGAs the concentration of boron is high. Thermal neutrons are the main cause of the problems in the integrated circuits due to interactions with the dopant boron

$$^{10}B + n \rightarrow^{7} Li + \alpha + \gamma(94\%) \tag{22}$$

$$\rightarrow^{7} Li + \alpha(6\%) \ . \tag{23}$$

As presented bellow, no permanent errors have been found in the board operation after irradiation with an 1 MeV equivalent neutron fluence of 4×10^{11} n/cm^2 and a gamma radiation dose of 150 Gy [34].

Due to event upsets the configuration memory of the software core inside

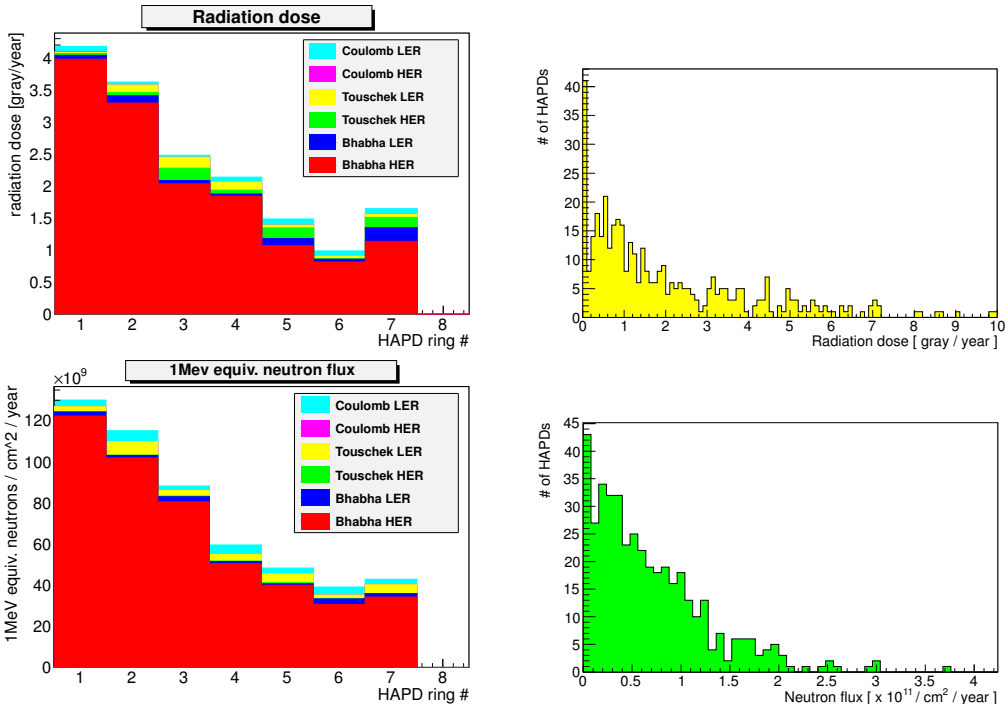


Figure 96: Expected radiation levels on the photon detector plane of the Belle II proximity focusing RICH with aerogel radiator. Radiation dose for different photon detector rings shown for different background contributing processes (upper left) can reach 70 Gy in ten years of operation. The distribution of photon sensors according to the expected radiation dose (upper right). The 1 MeV equivalent neutron flux for different detector rings shown for different background contributing processes (lower left) can reach 2×10^{12} of 1 MeV equivalent n/cm^2. The distribution of photon sensors according to the expected neutron flux (lower right).

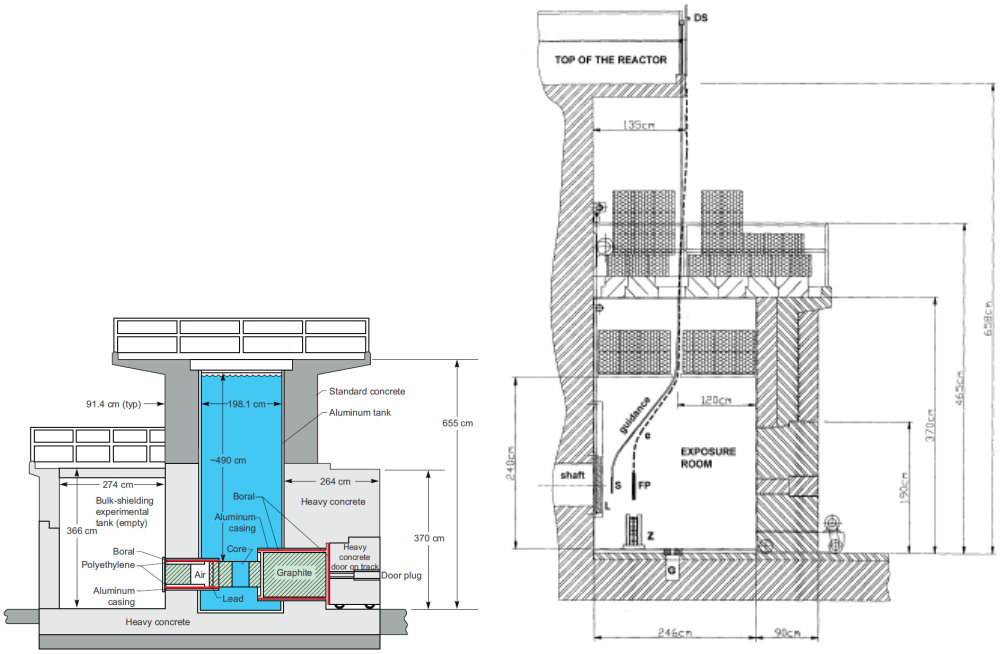


Figure 97: TRIGA Reactor: At the side of the reactor core the dry chamber allows irradiation of bigger samples. The samples can be mounted on a sledge and inserted in the measurement channel on the rails from the reactor top platform.

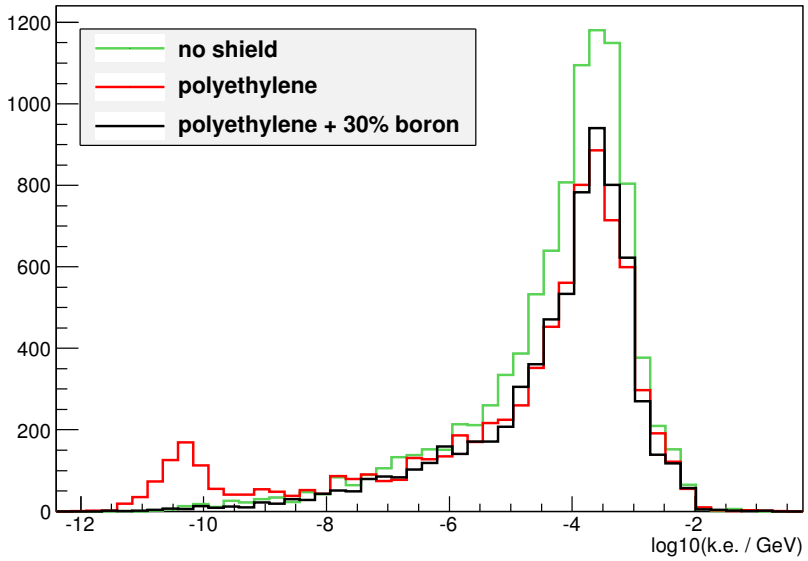


Figure 98: Neutron spectrum at the photon detector position [30]. The 6 cm polyethylene shield is added around the beam pipe to decrease the flux. Due to thermalization, the low energy part of the spectrum is considerably reduced. The thermal neutrons are absorbed by using borated polyethylene.

the FPGA is corrupted, which leads to malfunction in the operation of the board. By including the Soft Error Mitigation (SEM) controller [37], the majority of single bit flip errors can be corrected. We have monitored the operation of the SEM controller during irradiation with two different neutron fluxes. Although the expected neutron spectrum in the Belle II aerogel RICH (Fig. 136) differs from the reactor spectrum [35, 38](more thermal neutrons in the reactor), we assumed the same response and obtained upper limit values for the expected number of event upsets (Table 11). The data in the table are normalized to the expected neutron flux in the Aerogel RICH detector. Different numbers can be attributed to the dead time of the controller. During the data acquisition in the experiment, where the fluxes will be approximately 200 times lower, the SEM controller information will be used to reload the firmware in the FPGA, thus ensuring the correct operation of the electronics.

6.2.1 Experimental setup

The shielded experimental chamber of size of 2 m × 2 m× 2 m is positioned at the side of the reactor core. Its purpose is to enable the irradiation of bigger samples. Inside the experimental area there is a movable fission plate of radius of 25 cm, positioned 20 cm behind the rail which can be used for

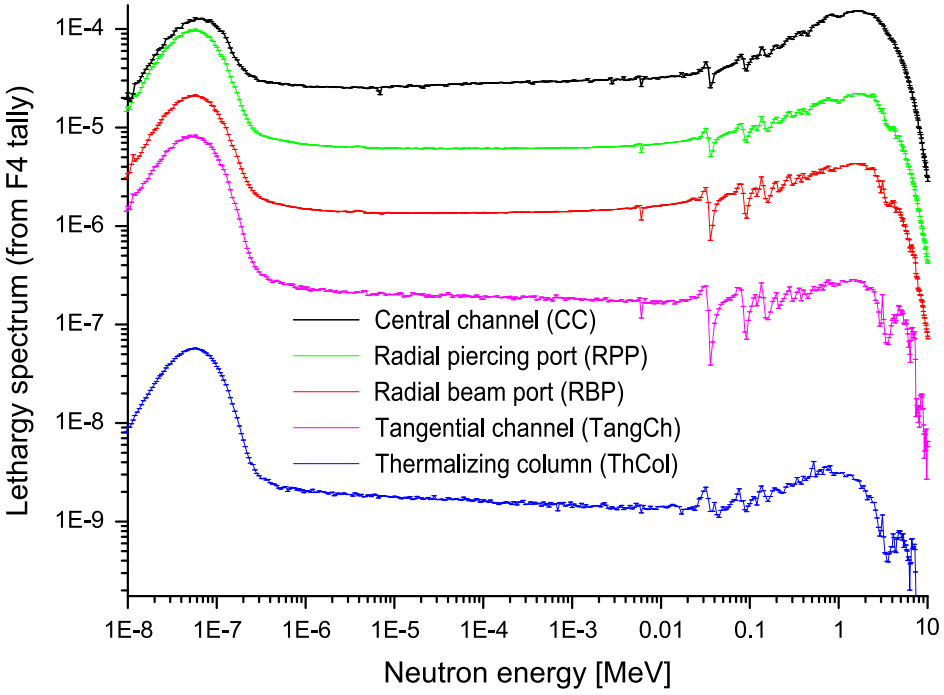


Figure 99: Neutron lethargy spectrum in the TRIGA irradiation channels [35]. The readout electronics was tested in the thermalizing column - ThCol. Note the correspondence between the lethargy and energy spectrum $\Phi_L = E\Phi_E$.

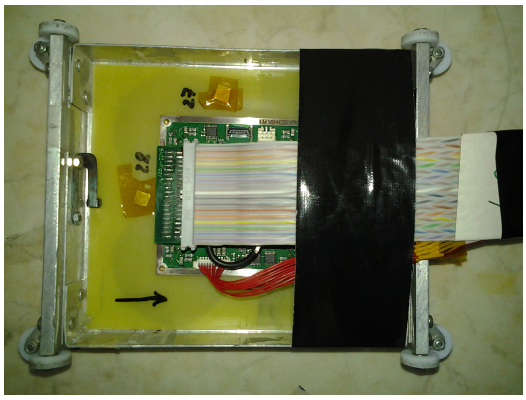


Figure 100: The readout board mounted on a sledge.

insertion and removal of the irradiation samples. A shutter between the rails and the reactor core is used to stop the radiation originating in the reactor core. The spectrum in the dry chamber is dominated by thermal neutrons (79%), the fission plate is used to provide slightly more fast (100 keV) neutrons (Fig. 99).

The readout board was mounted on a sledge (Fig. 100), that can be lowered from the top of the reactor to the irradiation position in the dry room. It was connected to other experimental equipment with 10 m long cables: twisted pair cable was used to connect the board to IO register VME CAEN V1495, flat cable was connected to the power distribution board, 2 coaxial LEMO cables were used for external monitoring of the signals and a JTAG flat cable was used for firmware upload and verification. The detection of erroneous operation was controlled by the PC installed outside the radiation area.

For calibration the doses were measured with two different dosimeters. The neutron flux of 3.275×10^6 1 MeV equivalent n/s/cm^2 was measured with two ELMA diodes mounted on the side of the board [39]. With such a flux the expected Belle II lifespan (1×10^{12} n/cm^2) could be reached in 85 h of readout electronics irradiation at full reactor power at a speed 700 $\times$ faster than in Belle II. The assumption is most probably not correct due to difference in neutron spectrum in Belle II and in the nuclear reactor as the effects of thermal and fast (300 keV) neutrons are different.

The radiation dose rate of 4.3 Gy/h was measured with 3 thermoluminescent dosimeters mounted on the side of the board. The radiation dose of 1 equivalent Belle II year is reached in one hour of irradiation at full reactor power.

Several tests have been made during several irradiation sessions in which the cumulative radiation dose reached a few Belle II lifetimes and the total neutron flux exceeded the equivalent of 4 Belle II years. During the test the boards were powered and constantly performing different checks:

- the ASIC chip configuration parameters were constantly verified;
- the threshold voltages (VTH1) were monitored,
- response of the readout board to different threshold voltages was recorded,
- the readout part was tested: test fixed data pattern was read instead of the ASIC channels,
- the temperature of the on-board sensor was measured,
- the verification of the firmware recorded the changes in the static part of the firmware.

The results of the checks were stored in the MySql database for further analysis.

6.2.2 Results

No hardware failure was found, all the components work after the firmware reload and operation of the board is normal. When the reactor power is switched off, the operation is normal.

When the reactor is operating at 250 kW changes in the configuration part of the firmware can be detected. To quantify the changes threshold scan curves were compared to the reference ones (Fig. 101) and the number of differences was recorded.

At lower fluxes the operation is normal. This might be due to the short measurement time. By increasing the reactor power the threshold scans show strange behavior. This may be induced by the changes in the ASIC configuration register. The tested version of the readout uses non radiation tolerant ASIC which will be in the final design replaced by the radiation tolerant successor.

The threshold voltage settings were measured externally with a multimeter and monitored during the operation. It was found that the settings were correct also at higher fluxes.

To locate the source of fault scans the firmware was modified to read the fixed data pattern. Such a modified firmware occupied 2% of the available space in the FPGA. The readout board was constantly read out and the number of fault reads have been counted. In the case the error was found the firmware was reloaded. At full reactor power we detected 9.2 errors/hour. For a fully occupied board this leads to about 460 errors/h (0.65 errors/ Belle II h). Although 420 readout boards will be installed in the Belle II, the boards will be individually re-flashed with a new firmware to meet the uninterrupted operation.

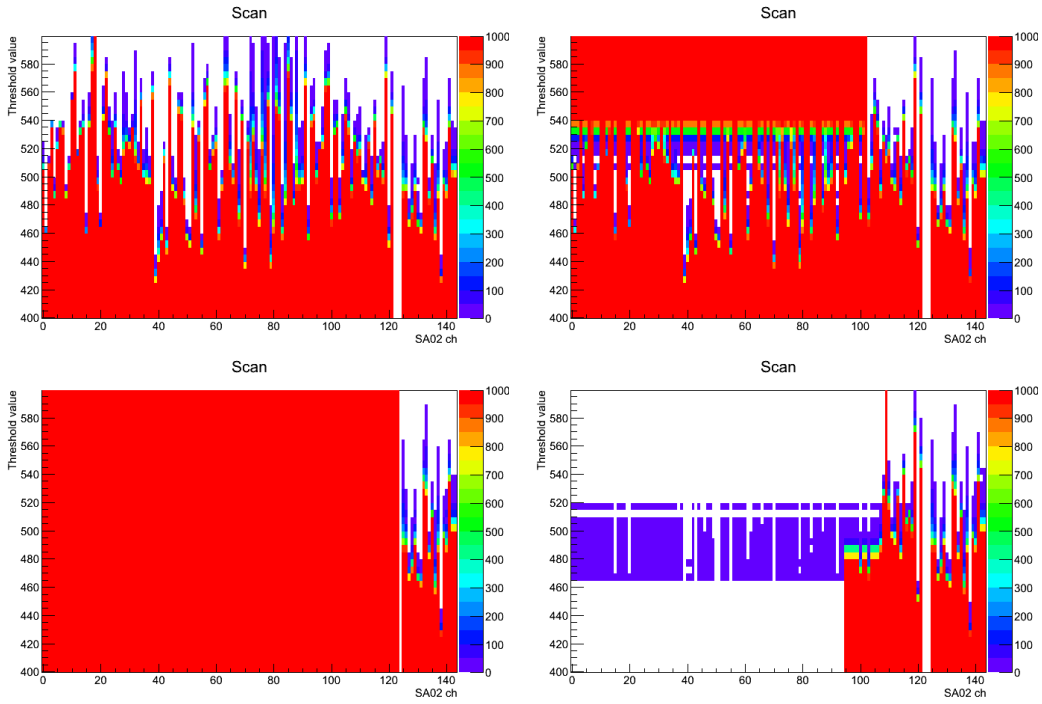


Figure 101: Errors during the data readout: normal scan (upper left), abnormal - the others. The errors mostly include wrong readout patterns for several or all channels.

6.2.3 Soft error mitigation controller

The readout board of the Firmware was modified to include the Xilinx Soft Error Mitigation (SEM) Controller. It is automatically configured, pre-verified solution to detect and correct unintended changes to the values stored in state elements caused by ionizing radiation (soft errors) in Configuration Memory of Xilinx FPGAs. It does not prevent soft errors, but it provides a method to better manage the system-level effects of soft errors. During the test the following procedure was executed:

- load the firmware,
- constantly check the serial output,
- once per minute inject test error,
- check the classification code FC,
- if SEM is left in the idle state switch to observation mode,
- if uncorrectable error is detected reload the firmware.

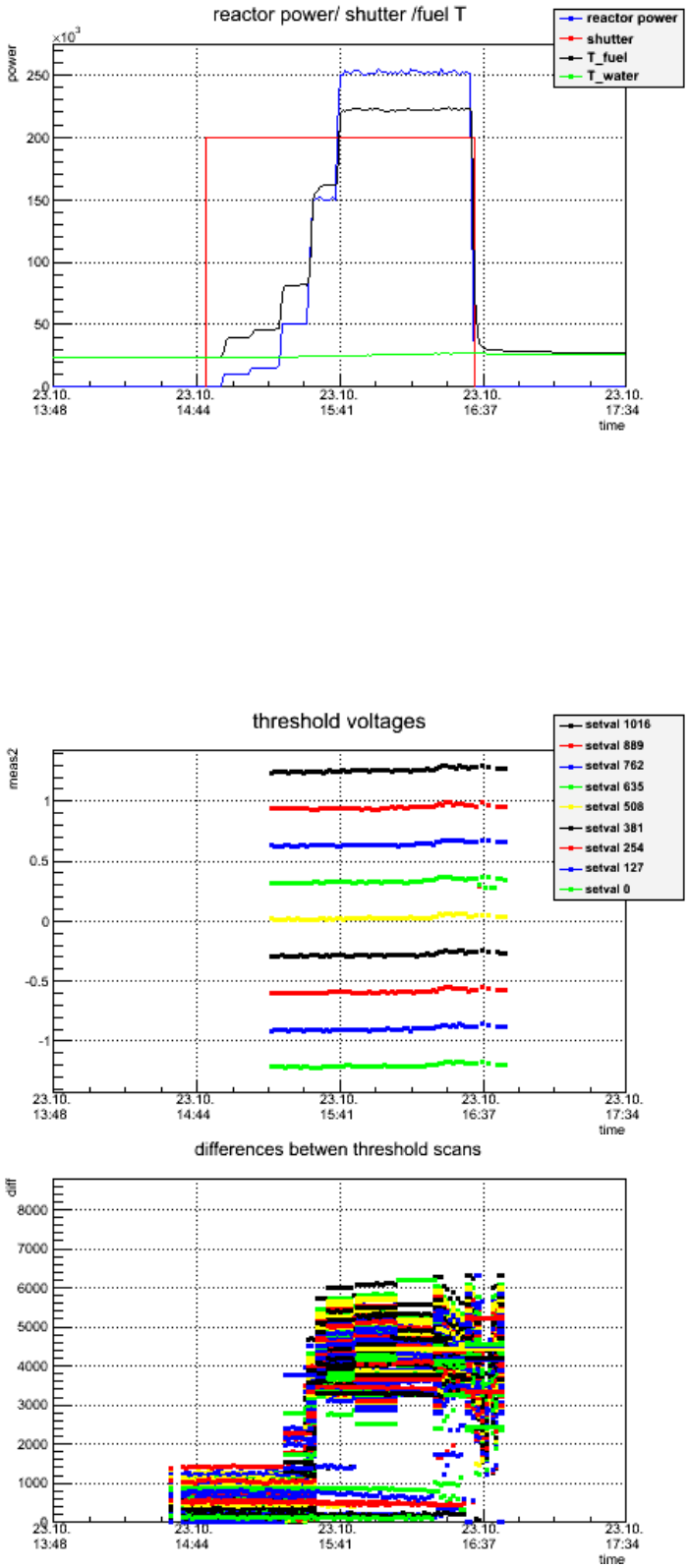


Figure 102: Operation of the readout board for different dose rates / reactor power: operational parameters of the reactor (upper), monitoring of the threshold voltages (middle), errors in the threshold scans (lower).

	SEU classification	10 kW	100 kW	100 kW wo fission
correctable non essential	FC 00	0.05	0.14	0.13
uncorrectable non essential	FC 20	0.1	0.04	0.07
Correctable essential	FC40 -SC10	5.06	3.4	3.53
Uncorrectable essential	FC60 -2*SC01	0.15	0.49	0.56

Table 11: Errors reported by SEM serial interface: expected Belle II aerogel RICH hourly rate of configuration errors extracted from the data during irradiation of the readout board with neutrons.

	N	t(min)	SEU/h	Belle II	SEU/h
SEM	nup	705	17	2488	7.5
SEM	ndown	20	17	70.5	0.2
no SEM	nup	832	21	2377	7.1
no SEM	ndown	30	21	85.7	0.3

Table 12: Results of the firmware read-back tests.

Several measurements at the reactor power of 10 kW and 100 kW were done. The analysis of the data coming from the serial interface allowed us to classify different types of events. As expected the single events upsets have been observed during the operation and the results are shown in Table 11.

From the acquired results it ca be concluded that expected rate in the Belle II environment is manageable. Software Error mitigation controller will correct most of the errors in configuration memory. For the uncorrectable errors the firmware will be reloaded.

6.2.4 Results of the firmware verification test at 100 kW

Another check was made with the firmwares with and without SEM controller. We have constantly read the firmwares from the readout board back to the computer through the JTAG interface and counted the number of differences with respect to the reference firmware.

In the Table 12 the number of bit transitions from 0 to 1 (up) and from 1 to 0 (down) is shown. The rate is approx. 1.5× the rate observed with the SEM controller through the serial interface. Note that there are considerably more transitions from 0 to 1 than from 1 to 0. This might be due to different occupancy of bits in the firmware. The rates of bit changes are the same for both types of firmware (Fig. 103). The reason for this is that the SEM stops working after it detects the uncorrectable error.

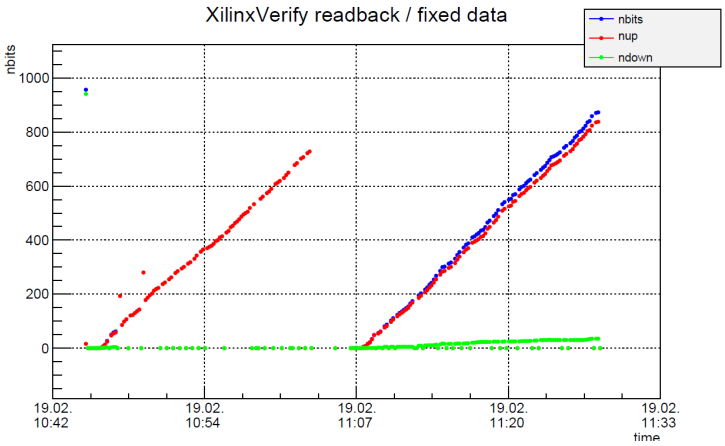


Figure 103: Number of bit differences for the firmware with SEM controller (left side of the chart) and the firmware without it (right side of the chart).

7 Beam test

A further, very important, verification of the performance of the ARICH detector was carried out by a test beam as a source of charged particles. The test took place at the Super Proton Synchrotron (SPS) accelerator experimental area at CERN in Geneva, Switzerland. SPS was designed in 1976 for proton experiments but later upgraded as the final injector for high-intensity proton beams for the Large Hadron Collider. The accelerator has a circumference of nearly 7 km and operates with beam energies up to 450 GeV. Operation as injector still allows continuation of the ongoing fixed-target research program, where the SPS is used to provide 400 GeV proton beams for a number of active fixed-target experiments. In the our test beam experiment, protons were used to produce pions in a conversion target. The control of the beam line allows to setup the energy and collimation of the test beam. For the present test, we have chosen a pion beam with a momentum of 120 GeV/c.

The experimental setup is enclosed in a light tight box where six HAPDs are mounted in the geometrical configuration as foreseen for the ARICH for Belle II. A schematic view of the setup is shown Figs. 138 and 105.

The beam test measurement setup was comprised of:

- Light tight box
  The light tight box houses the frame with HAPD sensors and front-end electronic boards. The distance between the aerogel and the detector plane was set to 20 cm.

- HAPD sensors and readout electronics.

- Tiles of aerogel.

- Tracking system composed of multi wire proportional counter chambers.
  In order to measure the entrance and exit point of the charged particle beam, two multi-wire proportional chambers (MWPC) are mounted on the light tight box on the outside. The active area of the chambers is about 50 mm $\times$ 50 mm.

- A VME readout system for data acquisition.
  A VME system housing the VME boards for reading the MWPCs and HAPDs.

- Triggering system composed of scintillators and photo multipliers.
  Two scintillators with photo multiplier tubes were placed in front and

behind the measurement setup along the particle track. A coincidence signal on both was used to trigger the DAQ system.

- Power supplies for HV.
- Power supplies for HAPD bias voltages.
- Power supplies for the electronics boards.
  Power supply boards are built with switching DC-DC converters in order to efficiently convert power and avoid additional heating inside the box.

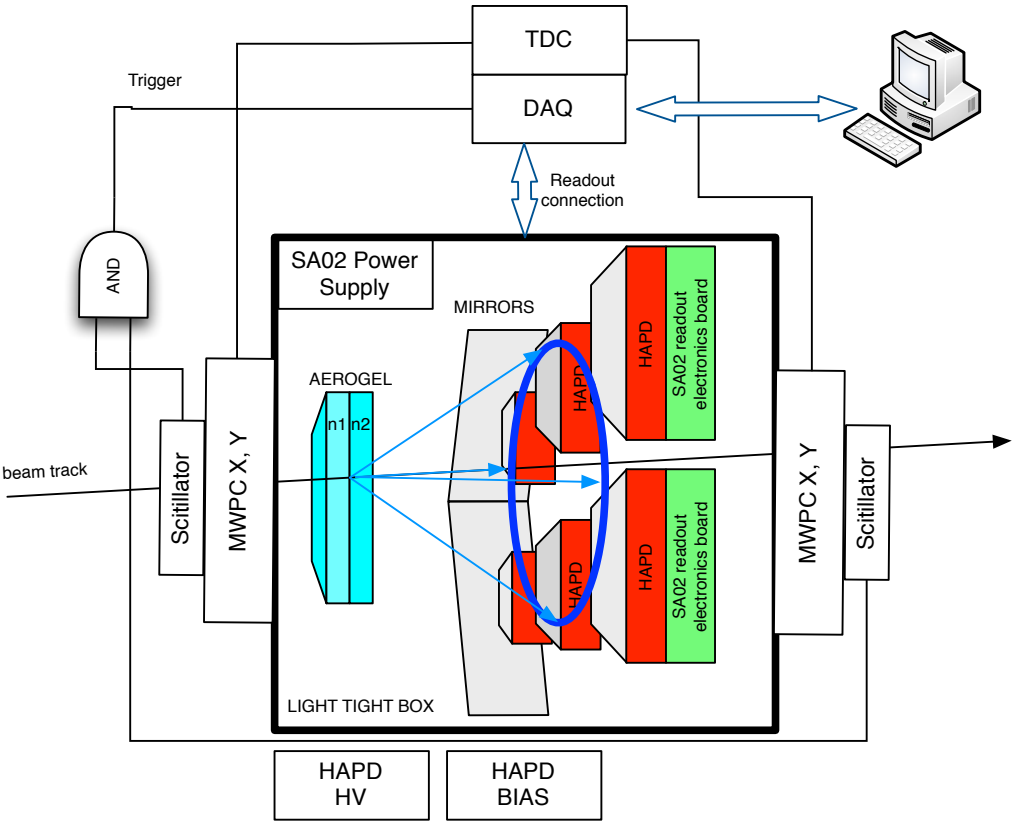


Figure 104: Beam test - schematic view of the setup.

The purpose of the beam test was to verify the new electronic readout, measure the number of detected photons per ring and the resolution per track. A number of different tests were therefore performed. Using two aerogels ($n_1 = 1.055$, $n_2 = 1.065$) in a focusing configuration we obtained a single photon Cherenkov angle resolution of $\sigma = 14$ mrad (Fig. 107). On average 11 photons per Cherenkov ring were detected. The results are consistent with expectations, and agree with results of previous beam tests [9]. The

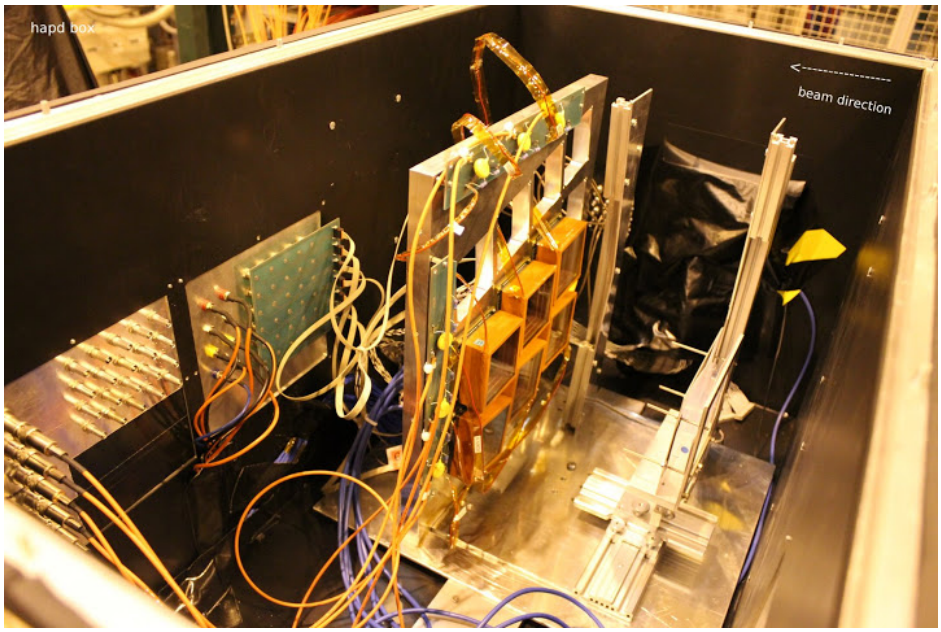


Figure 105: Beam test setup - photograph.

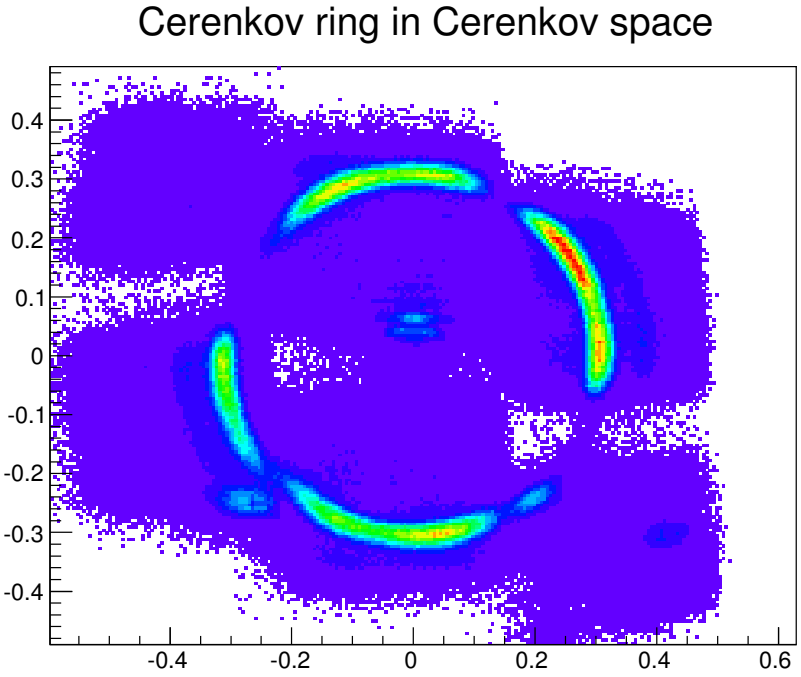


Figure 106: Beam test - accumulated hits on the photon detector, plotted in the Cherenkov space.

read-out electronics as discussed in this thesis performed very well, with a

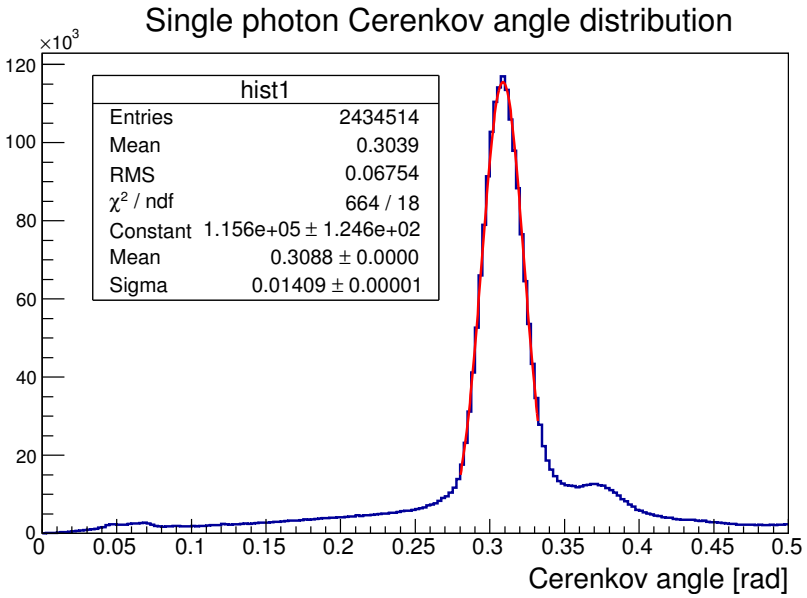


Figure 107: Beam test - Cherenkov angle distribution of recorded hits.

stable operation throughout the test.

8 Summary

The doctoral work focuses on the development of a suitable HAPD readout system for the proximity focusing RICH with aerogel radiator. The readout system has to operate in a radiation environment and in presence of 1.5 T magnetic field. A system which would satisfy these working conditions was designed, built and verified by the author with the collaborators of the Belle II ARICH group. The proximity focusing RICH with aerogel radiator, enables efficient separation of pion/kaons within the kinematic range 1 GeV/c to 4 GeV/c.

The Hybrid Avalanche Photo Detector was chosen as the photon detector of choice. The HAPD uses a Bialkali photocathode to convert photons into photo electrons which are accelerated along a HV potential. Within the ceramic frame of approximate $72 \cdot 72$ mm^2 four APD chips with 36 channels are placed. The accelerated electrons penetrate the APD chips creating additional avalanches. The outcome is about 40000 e^- per incident photon. The geometrical acceptance of the sensor is about 67 % with a pixels size of about 25 mm^2. The HAPD can operate in magnetic field and was tested to withstand the Belle II radiation environment. .

The readout system is composed of ASIC chips, an FPGA chip and additional circuits that allow the slow control of the readout parameters. The ASIC amplify, shape and discriminate detected signals on the HAPD. An ASIC chip has 36 channels and allows setting of shaping time, gain and offsets. In order to read an HAPD with 144 channels, four ASIC chips are used. The ASIC shaping time can be to set between 250ns and 1μs. This setting allows to optimize the signal to noise ration of the measurement. A numerical simulation of the ASIC signal path was made to better understand the signal behavior. Noise analysis indicate and equivalent nose charge of 1000e^- and 2000e^- for an irradiated HAPD using a shorter shaping time.

Digitized signals need to be processed before being sent to the DAQ system. A Spartan 6 FPGA from Xilinx company is used to record, store and transmit events. Moreover, the readout allows remote monitoring giving the possibility to remotely access the system and verify its operation. The readout electronics board that has all the described functionality is designed on a 12 layer PCB board. The size is about the same as the enclosure of the HAPD and fits compactly behind the HAPD sensor.

The firmware on the FPGA consists of three parts: the processor, the readout system and a single event upset mitigation controller. A processor is used for slow control communication and allows to setup the device. The readout system is made of shift registers and memory blocks which at trigger event store the data and sent them to the computer. Detection algorithms include the option to use edge or time over threshold detection. The single event upset mitigation controller is a part of the firmware that verifies the

integrity of FPGA while exposed to radiation. Detection algorithms include the option to use edge or time over threshold signal detection. In order to test the readout board under different operating conditions a setup was build which includes a VME system to transfer the data from the readout board to the computer.

Three measurement setups were made to verify the operation illuminating the HAPD with mostly single photons, a test in presence of 1.5 T magnetic field and a test under gamma and neutron exposure. Threshold scans of illuminated channels reveal a clear separation of single and multiple photons. Time over threshold technique is also investigated. By measuring the time of the signal being over a preset threshold an approximate value of detected photons per channel can be estimated.

The operation of the HAPD sensor and readout electronics were tested in presence of magnetic field. Both electronics and HAPD proved to be operational. Additionally the operation of the HAPD in presence of magnetic field improves slightly due a lower photoelectron backscattering from the APD surface and better trajectory of photo electrons at the edges inside the HAPD.

Xilinx reports on the vulnerability of their devices periodically. However the FPGA chosen has a drawback of being doped with Boron 10. This makes it more vulnerable to thermal neutrons as Boron decays into Lithium and releases an Alfa particle. At the Triga reactor, a department of Jožef Stefan Institute, the readout board was irradiated to cross verify its immunity. The outcome of the experiment shows an indication, that in Belle II environment each readout board will need a firmware reload after an hour of operation, what the group found to be acceptable. Moreover it confirmed that the SEU mitigation controller is able to notify the DAQ in case of firmware error.

Finally, a test in pion particles beam shows the system ability to measure Cherenkov rings. A mockup consisting of six HAPDs with corresponding readout electronics assembled in the final configuration was used to test the overall system performance in charged particle beam. Successive measurements included the verification of detection efficiency under angled tracks and the use of mirrors to verify the resolution in the outmost ring for the ARICH. The angle was fount to be 0.3 rad with the sigma of 14$m$rad. This includes systematic and statistical errors of the whole setup.

The presented readout needs to go trough another iteration where the readout board will be redesigned considering the correct cabling connectors. Moreover, at the time of writing, the group works on the development of a merger board to finalize the electronic equipment needed for the ARICH detector. The Aerogel Ring Imaging Cherenkov Detector is expected to be produced and installed by the year 2016 at KEK in Tsukuba, Japan.

9 Povzetek doktorskega dela

9.1 Uvod

Raziskave v fiziki visokih energij pogosto potekajo pri pospeševalnikih delcev. Tipični poskus poteka tako, da pospešeni delci trčijo med sabo ali v tarčo, ter opazujemo razpad njihovih produktov. Točka, kjer pride do interakcije se imenuje interakcijska točka, okoli nje pa je postavljen spektrometer. Spektrometer je kompleksna naprava sestavljena iz več detektorjev, ki merijo gibalno količino, energijo ali hitrost delcev. Podatki iz detektorjev se med eksperimentom sprotno shranjujejo v sistem za zajem podatkov. Ena pomembnejših nalog spektrometra je, da identificira delce. To pomeni, da določi maso teh delcev.

Za identifikacijo nabitih delcev v območju gibalne količine med 1 GeV/c in 100 GeV/c so zelo uporabni detektorji obročev Čerenkova. Detektor zgrajen na tej osnovi meri hitrost nabitih delcev. Za identifikacijo izmerjenega delca pa potrebuje še informacijo iz drugega detektorja, ki izmeri gibalno količino.

Na inštitutu KEK v Cukubi na Japonskem, mednarodna raziskovalna skupina raziskuje redke razpade B in D mezonov ter τ leptonov. Mezoni B so kratkoživi delci, ki razpadejo v pione, kaone, protone, neutrone, mione, elektrone ali gamma žarke in nevtrine. Eksperiment Belle je 10 letih izmeril 700 miljonov razpadov B^0 $\bar{B}^0$ [1]. Mednarodni raziskovalni skupini Belle je uspelo izmeriti majhno razliko v obeh razpadih. Meritev simetrije CP v sistemu B mezonov, ki sta jo izmerili neodvisni raziskovalni skupini Belle in BaBar (Stanford, ZDA [2]) sta potrdili napoved teoretičnih fizikov M. Kobayashi in T Maskawa. Za njun prispevek k znanosti sta leta 2008 prejela Nobelovo nagrado za fiziko [3].

Raziskovalna skupina Belle želi nadaljevati raziskave na približno 50 krat večjem vzorcu podatkov. To bo omogočeno z nadgradnjo trkalnika SuperKEKB in spektrometra Belle II na raziskovalnem inštitutu v Cukubi na japonskem.

9.1.1 Pospeševalnik KEKB

Pospeševalniki delcev so sestavljeni iz izvora nabitih delcev, linearnih pospeševalnikov ter sharnjevalnih obročev. Izvor elektronov je na primer lahko foto katoda. Pozitrone pa dobimo s trkanjem relativističnih elektronov v tarčo iz volframa. Pri tej reakciji se nekaj energije porabi za tvorbo parov elektronov in pozitronov. Za usmerjanje curka nabitih delcev se uporabljajo elektromagneti. Z njimi lahko ločimo nabite delce glede na njihov naboj. Prav tako lahko z njimi usmerjamo curek nabitih delcev v linearni pospeševalnik, ki jih pospeši do relativistične hitrosti z uporabo izmeničnega električnega polja znotraj resonančnih komor. Relativistični delci, so iz linearnega pospeševalnika preusmerjeni v shranjevalne obroče kjer krožijo v

časovno ekvididistantnih gručah. Število gruč v curku je določeno s frekvenco nihanja polja v resonančnih komorah in dolžino pospeševalnika. Shranjevalni obroči imajo prav tako resonančne komore, ki delcem dodajajo energijo izgubljeno zaradi sinhrotronskega sevanja in trkov.

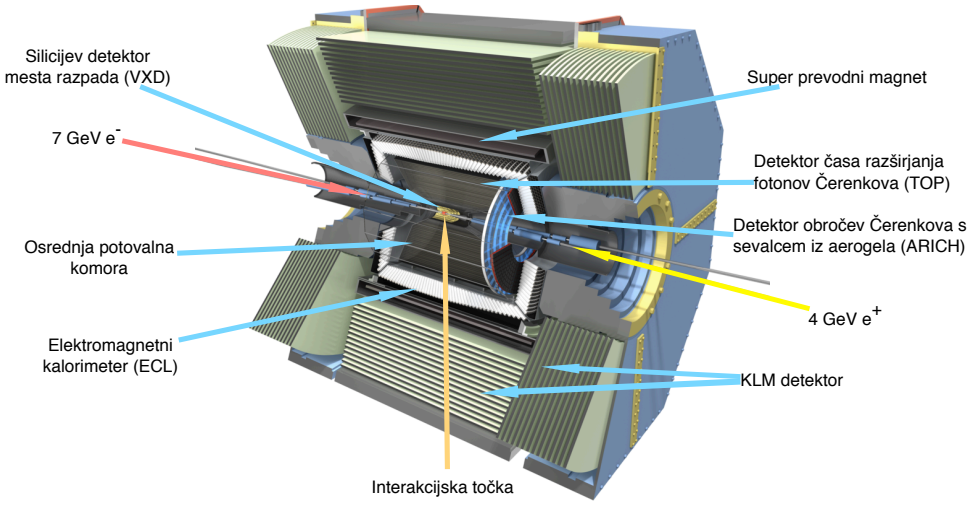
Pospeševalnik delcev KEKB pospešuje elektrone in pozitrone. Curka nabitih delcev se v interakcijski točki križata zato takšen pospeševalnik imenujemo trkalnik. Izbrana energija 8 GeV za elektrone in 3.5 GeV pozitrone sta izbrana tako, da ta sovpada z težiščno energijo E_{MC}=10.58 GeV resonance Υ(4S). Presek za tvorbo mezonov B je pri tej energiji relativno velik. V žargonu, se takemu pospeševalniku reče tudi tovarna B mezonov. KEKB je trenutno pospeševalnik z največjo luminoznostjo, ki znaša 2.11×10^{34} cm^{-2}s^{-1}.

Za nadaljevanje meritev trkalnik KEKB nadgrajujejo v SuperKEKB. Povečanje luminoznosti v trkalniku SuperKEKB bo omogočeno z znatnim zmanjšanjem površine žarkov v točki interakcije in s povčanjem toka v shranjevalnih obročih za elektrone in pozitrone.

9.1.2 Spektrometer Belle II

Spektrometer Belle II je hermetični detektor osnovnih delcev, postavljen okoli interakcijske točke trkalnika. Spektrometer predstavlja nadgradnjo spektrometra Belle in bo omogočil meritve razpadov na nadgrajenem trkalniku SuperKEKB. Spektrometer Belle II bo deloval v 20 krat večjem ozadju v primerjavi s prejšnjim eksperimentom. Ozadje izhaja iz sipanja žarka na residualih atomov plinov v cevi pospeševalnika, sinhrotronskega sevanja in visokega števila e^+ e^- ter $e^-e^+ \to e^-e^+\gamma$ dogodkov [5]. Prav tako naj bi se frekvenca izmerjenih dogodkov povečala za faktor 10 v primerjavi z predhodnim eksperimentom. To pogojuje nadgradnjo posameznih detektorjev in sistema za zajem podatkov. Spektrometer Belle II je sestavljen iz sledečih detektorjev (Slika 108):

- *Železnega jarma, ki služi kot ogrodje spektrometra in zaključuje magnetne silnice super prevodnega magneta.*
- *Super prevodni magnet z magnetnim poljem 1.5T;*
- *Detektor verteksov* - VXD;
- *Osrednja potovalna komora* - CDC;
- *Elektromagnetni kalorimeter* - ECL;
- *Detektor časa razširjanja fotonov Čerenkova* - TOP;
- *Detektor obročev Čerenkova s sevalcem iz aerogela* - ARICH;



Slika 108: Slika spektrometra Belle II v preseku.

- *Detektor mionov* - KLM;

Predstavil bom nekaj osnovnih zakonitosti sevanja fotonov Čerenkova, podal primere različnih detektorjev in predstavil smernice načrtovanja takega detektorja za spektrometer Belle II. Glavnino povzetka bom posvetil predstavitvi dokončne rešitve za čitalno vezje, ki bo vgrajeno v ta detektor. Za detektor obročev Čerenkova s sevalcem iz aerogela bom uporabljal kratico ARICH.

9.2 Detektor obročev Čerenkova s sevalcem is aerogela

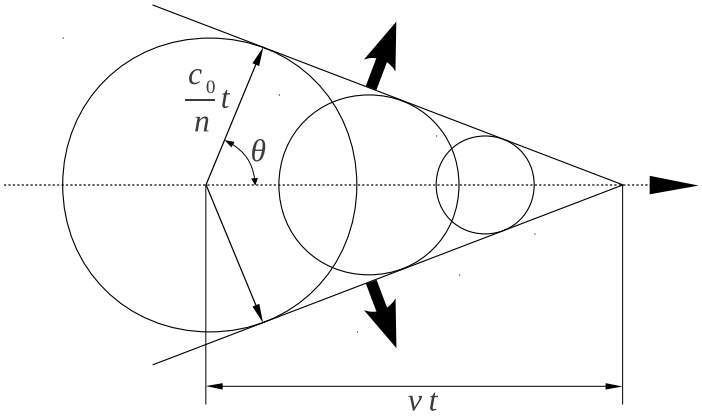
Detektorji obročev Čerenkova predstavljajo učinkovito orodje za identifikacijo nabitih delcev. Za spektrometer Belle II raziskovalna skupina načrtuje uporabo takega detektorja s sevalcem iz aerogela za merjenje hitrosti nabitih delcev v območju gibalnih količin med 1 GeV/c in 4 GeV/c.

9.2.1 Svetloba Čerenkova

Sevanje obročev Čerenkova predstavljajo fotoni, ki se izsevajo ko nabiti delec preleti medij z hitrostjo ki je višja od hitrosti svetlobe v tem mediju:

$$v > c_0/n \ , \tag{24}$$

kjer n predstavlja lomni količnik svetlobe v mediju, c_0 pa hitrost svetlobe v vakumu. Ruski znanstvenik Pavel Alekseyevič Čerenkov je prvi opazoval pojav in za njegov prispevek leta 1958 prejel Nobelovo nagrado za fiziko. Emisijo svetlobe povzroča lokalna polarizacija medija pri prehodu nabitega delca. Dipolne oscilacije rezultirajo v emisiji fotonov. V primeru, da je hitrost nabitega delca manjša od c_0/n, se prispevki dipolov destruktivno seštejejo. V nasprotnem primeru, ko je hitrost nabitega delca v mediju večja od hitrosti c_0/n pride do emisije elektromagnetnega vala kot posledice nihanja dipolov. V tem primeru se odziv dipolov sešteje konstruktivno [6]. Slika 109 prikazuje elektromagnetni val, ki prepotuje pot c_0t/n, medtem ko v tem času nabiti delec prepotuje pot $vt=\beta c_0$ upoštevajoč $\beta=v/c_0$. Kot izsevanih fotonov glede



Slika 109: Shematski prikaz kota sevanja fotonov Čerenkova.

na smer hitrosti (θ) je podana z :

$$cos\theta = \frac{1}{n\beta} \ , \tag{25}$$

kjer je maksimalni kot za β=1 podan z :

$$cos\vartheta_M = 1/n \ . \tag{26}$$

Število izsevanih fotonov na energijski interval in dolžino poti je izraženo z [7]:

$$\frac{d^2N}{dEdl} = \left(\frac{z^2\alpha}{\hbar c_0}\right)\left[1 - \left(\frac{1}{n(E)\beta}\right)^2\right] \ , \tag{27}$$

kjer $\alpha = \frac{e_0^2}{4\pi\varepsilon_0\hbar c_0} \approx \frac{1}{137}$ konstanta fine strukture.

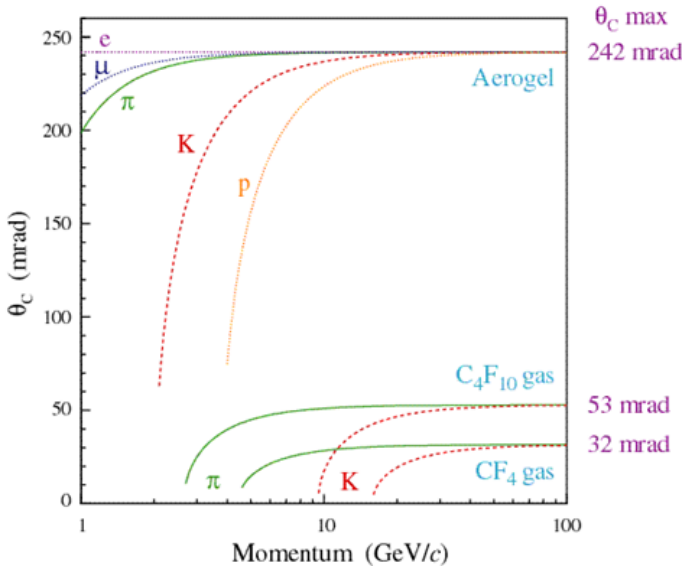
9.2.2 Detektor ARICH za spektrometer Belle II

Detektorji obročev Čerenkova so narejeni iz prosojnega sevalnega telesa s primernim lomnim količnikom, optičnega sistema (ekspanzijski volumen ali

zbiralna zrcala) in aktivne površine občutljive za posamezne fotone. Ločimo dva tipa detektorjev Čerenkove svetlobe; pragovne števce in detektorje, ki merijo kot Čerenkova. Oba principa imata skupne omejitve pri robnih pogojih delovanja. Gibalna količina nabitega delca mora biti večja od praga sicer ni izsevanih fotonov:

$$p_{prag} = \frac{mc}{\sqrt{n^2 - 1}} \ . \tag{28}$$

Lažji delci imajo nižji prag, kar omogoči ločevanje.

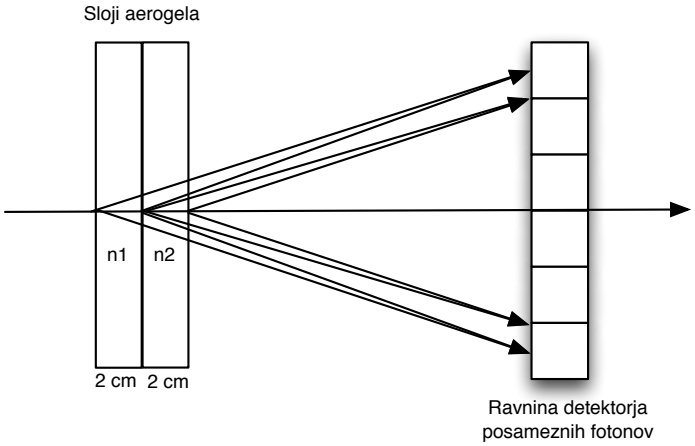


Slika 110: Kot izsevanih Čerenkovih fotonov kot funkcija gibalne količine za različne sevalce. Primer za plinski in trdni sevalec.

Z uporabo sevalcev različnih lomnimi količnikov je možno prilagoditi območje željene gibalne količine. Poleg pragovnega števca se uporablja tudi detektor, ki meri kot izsevanih fotonov Čerenkova glede na smer hitrosti delca. Detektor s takšno geometrijo bo uporabljen v spektrometru Belle II. Za pokrivanje prostorskega kota v smeri gibanja težišča razpadlih delcev, so v raziskovalni skupini Belle II predvideli detektor obročev Čerenkova s sevalcem iz aerogela. Geometrija detektorja, ki bo zamenjal pragovni števec v spektrometra Belle (v smeri naprej) je prikazana na sliki 111.

Napake pri meritvi emisije fotonov Čerenkovega kota prispevajo:

- ločljivost meritve pozicije zadetka fotona na detektorski ravnini,
- kvaliteta optičnega sistema,
- napake pri meritvi sledi nabitega delca,
- in večkratno sipanje fotona v sevalcu.



Slika 111: Detektor obročev Čerenkova v fokusirani konfiguraciji.

Takšen detektor je omejen s pragom gibalne količine in resolucijo s katero lahko izmerimo kot izsevanih fotonov Čerenkova pri velikih gibalnih količinah. Poleg naštetega je faktor, ki določa delovanje takšega detektorja tudi število zaznanih fotonov v obroču. To je podano z:

$$N_{det} = L \int Ts(E) \cdot \epsilon(E) \cdot T_e \cdot \frac{d^2 N_c}{dE dL(E)} dE \ , \tag{29}$$

kjer je L dolžina sevalca, Ts(E) transmisijski faktor sevalca , ϵ(E) produkt kvantnega in zbiralnega izkoristka senzorja za posamezne fotone, T_e izkoristek čitalne elektronike in $\frac{d^2 N_c}{dE dL(E)}$ število izsevanih fotonov na energijski interval fotonov na poti delca skozi sevalec podano z Eq. 27. V detektorju ARICH je kot sevalec uporabljen aerogel. V proizvodnem procesu aerogela je možno proizvesti različne lomne količnike med 1.01 in 1.1. Aerogel je prosojen materjal z fino silicijevo strukturo in zračnimi žepki velikostnega reda nekaj nm. Aerogel je prikazan na sliki 112 [9]. Ključni parameter, ki določa točnost meritve Čerenkovega kota za nabiti delec, je tudi število fotonov N_{det} , ki jih zaznamo v obroču:

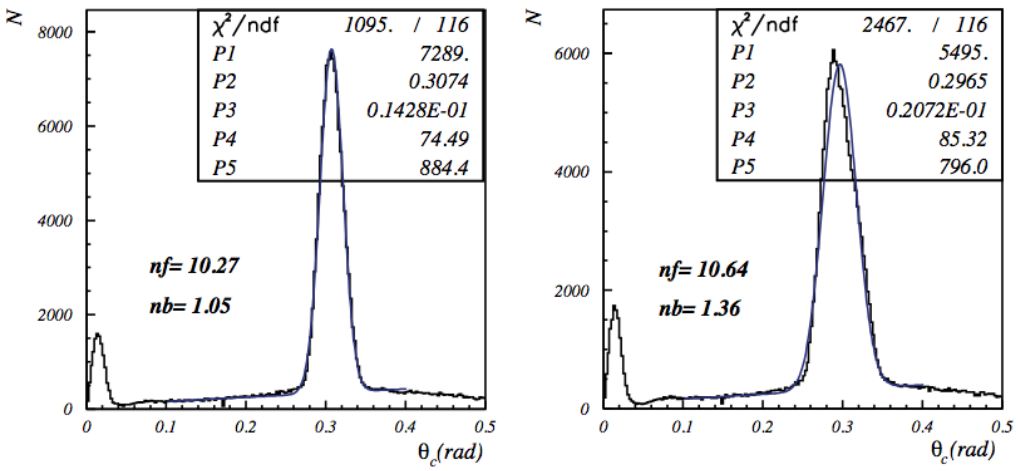
$$\sigma_{sledi} = \sigma_\theta / \sqrt{N_{det}} \ . \tag{30}$$

Debelejši sevalec poveča število izsevanih fotonov, a ob enem tudi poveča nedoločenost emisijske točke fotonov in s tem poslabša natačnost meritve kota Čerenkova. V fokusirni konfiguraciji detektorja ARICH sta uporabljena 2 sloja aerogela. Lomna količnika za aerogela sta izbrana tako, da obroča fotonov iz prvega in drugega sevalca na detektorski ravnini sovpadata. S tem ohranimo število izsevanih fotonov v obroču ob zmanjšani napaki zaradi nedoločenosti emisijske točke. Za detektor obročev Čerenkova v fokusirni konfiguraciji sta predvidena dva aerogela debeline 2 cm z lomnima količnikoma $n_1 = 1.046$ in $n_2 = 1.056$. Ekspanzijski volumen je dolg 20 cm, predvidena

površina občutljivega površinskega elementa (piksla) senzorja fotonov pa 25 mm^2 [9].

Slika 112: Aerogel [9].

V curku nabitih delcev je raziskovalna skupina izmerila delovanja detektorja v fokusirni geometriji. V preizkusu je uporabila enoslojni aerogel debeline 4 cm z lomnim količnikom n=1.046, kar da v povprečju 10.6 fotonov na Čerenkov obroč pri σ=20 mrad. V konfiguraciji z dvema slojema aerogela debeline 2 cm vsak in lomnima kolčnikoma n_1= 1.046 in n_2 = 1.056 pa 10.3 fotonov na Čerenkov obroč in σ=14 mrad.



Slika 113: Primerjava Čerenkovega obroč za 2 plastni aerogela (n_1= 1.046, n_2 = 1.056 : 2 × 2 cm), in enoplastni aerogel debeline 4 cm [9].

Razlika v Čerenkovem kotu za pione in kaone pri 4 GeV/c znaša 23 mrad. Sposobnost ločevanje med delci lahko izrazimo kot $\frac{\Delta\theta_c}{\sigma_\theta}\sqrt{N_{det}}$, kjer je $\Delta\theta_c$ razlika v Čerenkovem kotu med pioni in kaoni. To omogoča učinkovito ločevanje

pionov in kaonov z $\approx 5\sigma$ natančnostjo. Ob poznavanju gibalne količine za delec lahko izračunamo njegovo maso po enačbi p=$\beta\gamma$mc.

9.3 Senzor za posamezne fotone in čitalna elektronika

Senzor za zaznavanje posameznih fotonov predstavlja eno izmed ključnih komponent za detektor ARICH. Detektor za delovanje potrebuje pozicijsko občutljiv senzor posameznih fotonov v območju valovne dolžine 100 nm $\leqslant \lambda \leqslant$ 1000 nm. Za uporabo v spektrometru Belle II mora senzor učinkovito delovati v prisotnosti magnetnega polja 1.5 T, imeti mora zadostno pozicijsko ločljivost in vzdržati povečane vrednosti sevanja gamma in nevtronov.

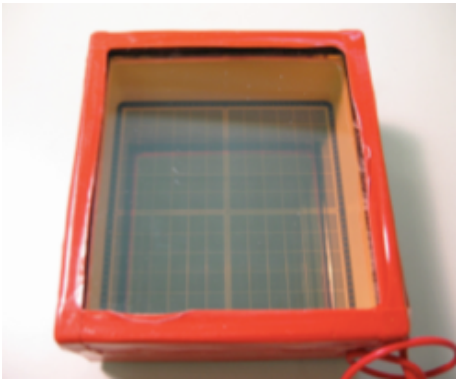
Parametri, ki določajo kvaliteto senzorja za posamezne fotone so [12]:

- *Kvantni izkoristek, ki predstavlja povprečno število generiranih foto elektronov na vpadni foton.*
- *Zbiralni izkoristek, ki je razmerje zbiralne površine s celotno površino okna naprave.*
- *Ojačanje, ki predstavlja število zbranih elektronov na generirani fotoelektron.*
- *Temni šum, ki predstavlja signale brez osvetlitve.*
- *Dinamično območje, ki je določeno z najmanjšim in največim signalom iz naprave.*
- *Časovni odziv, ki predstavlja povprečni čas, ki je potreben za pretvorbo upadlega fotona v elektični signal.*
- *Mrtvi čas predstavlja čas med dvema dogodkoma brez nalaganja signalov.*

9.3.1 Senzor za posamezne fotone HAPD

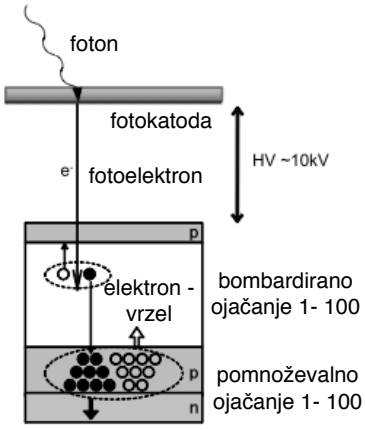
Raziskovalna skupina se je odločila uporabiti hibridno plazovno foto diodo (HAPD) podjetja Hammamatsu photonics. Senzor združuje princip delovanja foto pomnoževalke in plazovne foto diode. Senzor HAPD sestavljajo keramično ohiše velikosti 72 mm × 72 mm × 30 mm , vstopno okno iz kvarčnega stekla na katerega je naparjena Bi-Alkali foto katoda, in štirje čipi segmentirani na posamezne plazovne fotodiode. Senzor HAPD ima skupno 144 aktivnih pikslov velikosti 4.9 mm × 4.9 mm (Slika. 114).

Foton, ki prodre skozi okno iz kvarčnega stekla se pretvori v fotoelektron s kvantnim izkoristkom 25% (Slika. 115). Med fotokatodo in plazovnimi foto diodami je napetostni potencial med 7 in 10 kV, ki izbite fotoelektrone

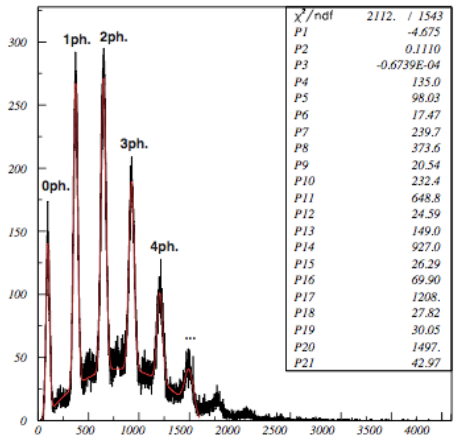


Slika 114: Slika senzorja HAPD

pospeši proti plazovnim foto diodam. Elektroni prodrejo v piksle plazovnih fotodiod in tam ustvarijo približno 3000 parov elektron-verzel. Na plazovno foto diodo je priključena napetost v zaporni smeri, ki povzroči nadaljnje pomnoževanje signala. Tipično za en foton zberemo približno 10 fC naboja. Zbiralni izkoristek HAPD je 67% [9]. Senzor HAPD tako omogoča učinkovito merjenje posameznih fotonov(Slika. 116) . Porazdelitev naboja za posamezne fotone je prikazana na sliki 116



Slika 115: Princip delovanja senzorja HAPD.



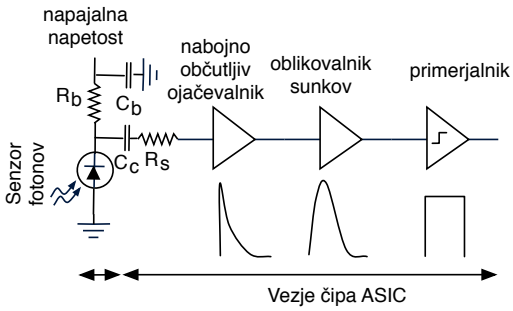
Slika 116: Porazdelitev naboja za posamezne fotone.

9.3.2 Čitalna elektronika za senzor HAPD

Predstavil bom dokončno rešitev čitalne elektronike za senzor HAPD, ki bo uporabljena v detektorju ARICH v spektrometru Belle II. Čitalna elektronika za senzorje posameznih fotonov bo vgrajena v samem spektrometru,

kjer je na razpolago zelo malo prostora, saj ga večino zavzema ekspanzijski volumen detektorja. Čitalna elektronika mora samostojno in učinkovito delovati pod enakimi pogoji kot senzor posameznih fotonov HAPD. Poleg zajema podatkov mora čitalna elektronika podatke ustrezno procesirati in ob signalu za proženje dogodka poslati v sistem za zajem podatkov spektrometra. Omogočiti mora tudi možnost opazovanja analognih signalov in delovnih napetosti ter sprotno preverjanje pravilnega delovanja. Zasnova čitalne elektronike temelji na integriranih vezjih za specifične namene (ASIC) ter programabilnem vezju (FPGA). Dodatne vgrajene komponente skrbijo za nastavitve nivoja diskriminacije in nadzor vezja.

Čipi ASIC so pogosto uporabljeni v instrumentacijski merilni napravi. Za zajem signalov iz senzorja HAPD smo uporabili čip ASIC, ki so ga razvili v japonski vesoljski agenciji JAXA [13]. Čip je izdelan v 35 μm tehnologiji na silicijevem substratu in ima 36 merilnih kanalov v ohišju velikosti 13 mm $\times$ 13 mm. Za pokrivanje vseh 144 pikslov HAPD senzorja jih potrebujemo 4. Vsak kanal je sestavljen iz nabojno občutljivega ojačevalnika, oblikovalca signala in enobitnega digitalizatorja. Izhodni signal predstavlja binarni izhod, ki je po dolžini enak času, ki ga analogni signal preživi nad pragom (Slika 117). Delovanje čipa ASIC lahko tudi nastavimo. Nastavitve za vse kanale omogočajo izbiro ojačanja signala in oblikovanja sunkov τ. Vrednosti τ se lahko izbere med 250 ns in 1 μs. To omogoča optimizacijo razmerja med signalom šumom za senzorje skozi življenjsko dobo eksperimenta.



Slika 117: Konstrukcija ojačevalnika in digitalizatorja za posamezni kanal v čipu ASIC.

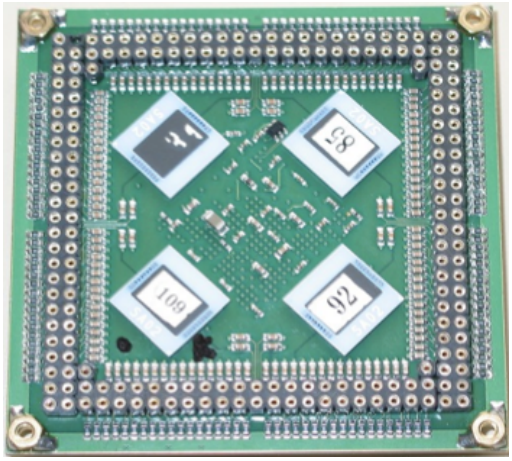
Na posameznih kanalih znotraj ASIC čipa je mogoče premikati srednje vrednosti kanala v 15 korakih po 40 mV in 15 korakih po 4 mV za vsak kanal. Izhodi čipov ASIC so vezani na vezje FPGA . FPGA vezja so programabilna vezja sestavljena iz nastavljivih logičnih blokov in povezovalnih kanalov, ki omogočajo realizacijo poljubnih binarnih operacij. Vezje FPGA smo uporabili za procesiranje signalov iz čipov ASIC in za izgradnjo logičnih operacij, ki omogočajo komunikacijo z zunanjim svetom. Za našo čitalno elektroniko smo izbrali FPGA XC6SLX45 podjetja Xilinx [17]. Pri izbiri smo se osredotočili na fizično velikost integriranega vezja, razpoložljivo programabilno

logiko in zadostno procesno hitrost.

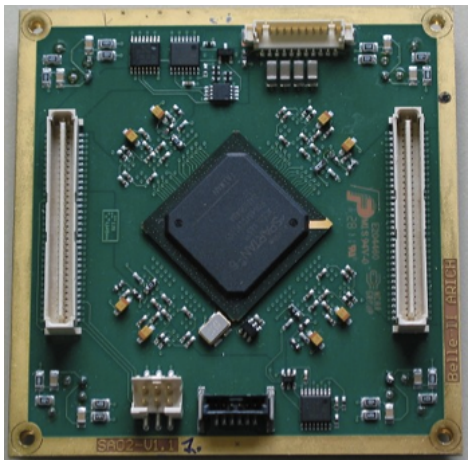
Za dodatno periferno podporo pri zajemu podatkov smo izbrali:

- *Digitalni potenciometer, ki omogoča nastavitev napetosti praga proženja signala ASIC [19].*
- *Analogni multiplekser, ki omogoča vpogled v delovanje ojačevalnika znotraj ASIC vezij in verifikacijo napajalnih napetosti [21].*
- *Vezje za generiranje testnih signalov, ki je sestavljeno iz digitalnega potenciometra in digitalnega stikala [19, 23].*
- *Termometer [22].*

Elektronsko vezje, ki bo omogočilo zajem podatkov iz senzorja HAPD je sestavljeno iz zgoraj naštetih komponent (Sliki 118 in 119). Za izdelavo tiskanega vezja smo uporabili računalniški program Altium designer [26]. Najprej smo izrisali komponente, nato shematične načrte in iz njih tiskano vezje. Gre za kompleksno tiskano vezje narejeno iz 12 slojev, ki po velikosti sovpada z senzorjem HAPD. Čitalno elektroniko se priključi na zadnjo stran senzorja (Slika 120). Čitalna elektronika ima številne priključke za napajanje senzorja HAPD, priključitev napajanja za elektroniko, servisni priključek za nalaganje programov in 2 razširitvena priključka za povezavo z zunanjim svetom. Končna poraba vezja ne presega 1 W.

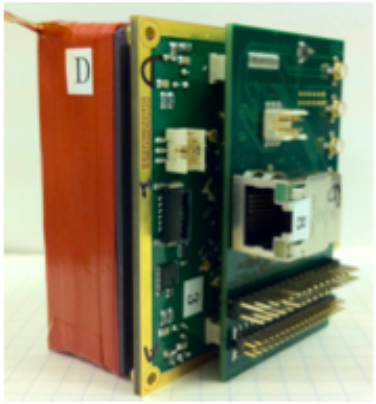


Slika 118: Čitalna elektronika, 4 čipi ASIC in priključek za senzor HAPD.



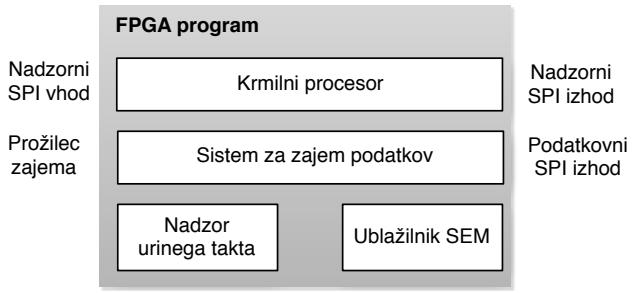
Slika 119: Čitalna elektronika, FPGA vezje in priključki za komunikacijo z zunanjim svetom.

Čitalna elektronika za senzor HAPD predstavlja visoko integrirano vezje. Za svoje delovanje potrebuje nadzorni sistem za upravljanje z posameznimi



Slika 120: Senzor HAPD priključen na čitalno elektroniko.

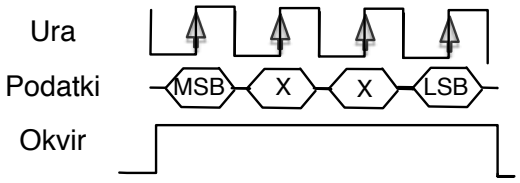
podsistemi in sistem, ki skrbi za zajem podatkov. Tako konfiguracijo imenujemo sistem na čipu (SoC). Program za vezje FPGA vsebuje procesor za nadzor delovanja ter sistem za zajem podatkov. Za pravilno delovanje sta potrebna še dva podporna sistema. To sta sistem za nadzor urinega takta in vezje za ublažitev napak pri sevalnih poškodbah integritete programa (Slika 121).



Slika 121: Shematični prikaz arhitekture programa na FPGA vezju.

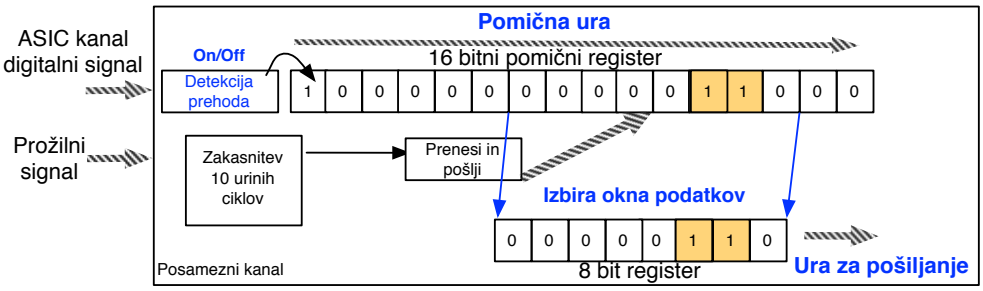
Na programabilnem vezju FPGA smo implementirali krmilni procesor. Slednji služi kot vstopna točka iz zunanjega sveta in poenostavi nastavitve različnih naprav z generičnim pristopom za vse nastavitve. Procesor je sestavljen iz sprejemnika, krmilnika in namenskih gonilnikov. Integriran na FPGA vezju zmanjša količino potrebnih povezav in poenostavi komunikacijo. Naprave, kot so nastavitve praga proženja, ASIC čipi in temperaturni senzorji, omogočajo povratno informacijo v nadzorni sistem preko ločenega vodila. Procesor za komunikacijo z zunanjim svetom uporablja protokol SPI. Primer take komunikacije je prikazan na sliki 122.

Digitalizirane signale iz ASIC čipov je potrebno zaznati in poslati v sistem za zajem podatkov. Na FPGA vezju smo razvili sistem za merjene, ki omogoča 3 principe zajema podatkov. To so; beleženje signala ob prehodu



Slika 122: Primer SPI komunikacije za prenos 4 bitnega sporočila.

čez prag, meritev dolžine signala nad pragom ter sistem za verifikacijo integritete podatkov. Slednji na vseh kanalih izpisuje fiksno vrednost in služi za diagnostiko prenosa podatkov. Čitalni sistem ima nekaj skupnih parametrov. Za beleženje signalov iz ASIC čipov je v FPGA-ju vgrajen 16 bitni pomični regiester za vsak kanal (Slika 123). Princip delovanja je sledeči. Signal iz

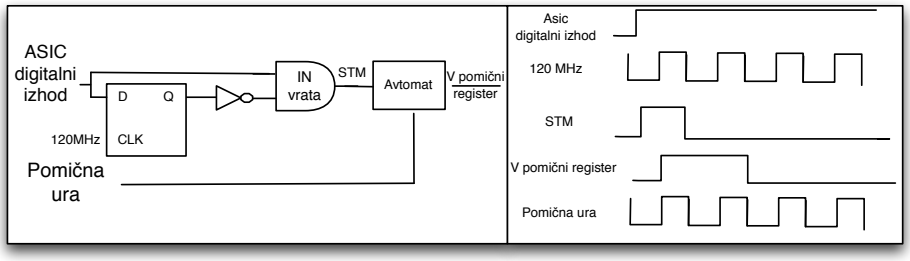


Slika 123: The data sampling and transmission.

ASIC čipa potuje po pomičnem registru. Frekvenco pomika lahko nastavimo med 3.75 MHz in 48 MHz. Sistem se samodejno sproži 10 urinih ciklov po prihodu prožilca. Takrat se podatki v pomičnem registru prenesejo v 8 bitni register za pošiljanje podatkov. V naslednjem koraku se podatki prenesejo iz čitalne elektronike v zunanji sistem. Za boljšo časovno korelacijo med signalom in proženjem omogoča sistem izbiro, katerih 8 bitov bo prenesenih v register za pošiljanje. Register za pošiljanje ima prav tako nastavljivo uro. Največja hitrost prenosa omogoča pošiljnaje podatkov pri 120 MHz uri, kar omogoča, da se 8 bitni podatki za vseh od 144 kanalov prenesejo v 11 μs.

Če želimo sistem uporabiti na način, da bo zaznaval samo prehode je potrebno med ASIC čipe in pomočne registere vključiti vezje za detekcijo prehodov. Vezje je prikazano na sliki 124. Vhodni signal je na FPGA vezju primerjan z 120 MHz uro. V kolikor pride do prehoda, bo vezje prožilo signal, ki aktivira sekvenčni avtomat. Avtomat bo sinhrono s taktom ure pomičnega registra vpisal dva bita v pomični register in se vrni v osnovno stanje zajema.

Proizvajalec FPGA čipov ponuja programsko okolje s katerim se izdela program za delovanje čipa. Znotraj tega okolja ponuja tudi nekaj generičnih modularnih rešitev. Uporabili smo modul za urejanje urnih taktov in kontroler, ki pregleduje integriteto programa na FPGA vezju.



Slika 124: Princip delovanja zajema podatkov za beleženje prehodov.

Modul, ki ureja urni takt vezja zaprtozančno krmili željene vrednosti urinih ciklov na vezju in s tem poveča robustnost vezja zaradi variacij napajalnih napetosti ali ob spremembi temperature. Modul skrbi tudi za sofazno usklajenost urinih ciklov znotraj FPGA vezja. Drugi modul se imenuje ublažitveni (SEM) krmilnik. Integrirana vezja na osnovi silicija so občutljiva na sevalne poškodbe. Pri prehodu nabitega delca se lahko inducira zadosten naboj, da logičnemu vezju spremeni vrednost. Krmilnik SEM omogoča pregledovanje vezja FPGA med delovanjem. Manjše napake lahko odpravi, v primeru poškodbe osnovnega programa pa odkrito napako javi preko serijskega vodila. SEM krmilnik ne preprečuje napak pač pa predstavlja učinkovito orodje za odkrivanje posameznih sevalnih dogodkov znotraj vezja FPGA.

Čitalna elektronika za senzor HAPD je s tem končana. Za preizkus delovanja je potrebno vezje priključiti na sistem za zajem podatkov. V naslednjem pod poglavju bom predstavil tak sistem.

9.3.3 Sistem za zajem podatkov

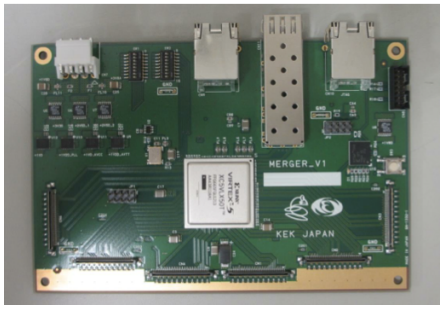
Sistem za zajem podatkov je vez med čitalno elektroniko in računalniško podprtim sistemom, ki beleži podatke. Odločili smo se, da tak sistem sestavimo na osnovi VME standarda [27] in uporabimo digitalni vhodno izhodni register CAEN VME 1495 [28]. CAEN VME 1495 je sestavljen iz dveh FPGA vezij (Slika 125). Prvo FPGA vezje je tovarniško programirano za komunikacijo z VME vodilom. Drugo FPGA vezje pa omogoča uporabniku izdelavo poljubne arhitekture programa. Sistem za zajem podatkov je sestavljen iz:

- Procesorja, ki bere VME registre in pošilja ukaze na čitalno elektroniko preko SPI vodila.
- Registra za zajem podatkov. Pomični register sprejema sveže podatke iz čitalne elektronike in rezultat prenese na VME vodilo.
- Veto vezje skrbi za zajem podatkov. Pri zajemu odloča kateri prožilni signal bo sporožil zajem na čitalni elektroniki. Po zajemu obvesti

računalniški sistem o prihodu svežih podatkov in se resetira po branju. Za tem se cikel ponovi.

Slika 125: Shematski prikaz priključitve čitalne elektronike vhodno izhodnega registra CAEN 1495 v sistemu za zajem podatkov.

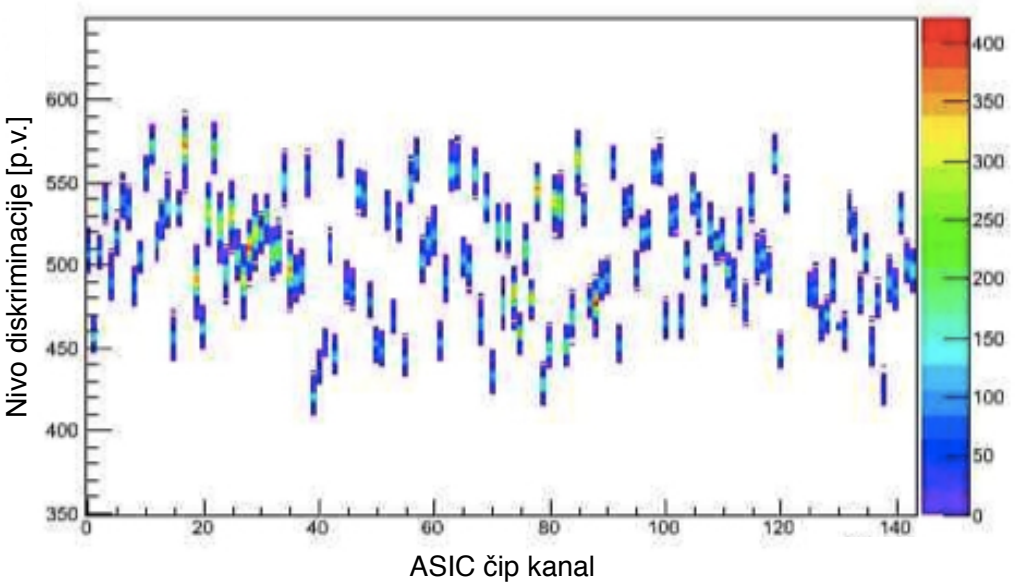
CAEN VME 1495 register omogoča priključitev do 4 module čitalne elektronike za HAPD senzorje. Zasnova čitalnega sistema na takšni osnovi je bila izbrana zaradi kasnejše vgradnje čitalne elektronike v detektor obročev Čerenkova. Za uporabo čitalne elektronike v detektorju je predvideno dodatno elektronsko vezje [15]. To dodatno elektronsko vezje za delovanje uporablja zmogljiveši FPGA Virtex 5 in njegova naloga je, da krmili in shranjuje podatke iz 4 do 6 čitalnih vezij (Slika. 126). Ob dogodku, se podatki prenesejo iz čitalnih vezij, se združijo in pošljejo po optični povezavi do sistema za zajem podatkov spektrometra. Procesorska moč, ki je na razpolago zadostuje za izgradnjo nadaljnjih algoritmov za izboljšavo zajema in proženja.



Slika 126: Merger board

9.3.4 Laboratorijski preizkusi delovanja čitalne elektronike

Čitalno elektroniko smo preverili v laboratoriju. Preizkus vključuje verifikacijo pravilnega odziva vseh strojnih komponent in algoritmov. Manjše napake smo odpravili in potrdili pravilnost delovanja. Običajno se preizkus detektorja vrši z meritvijo odziva detektorja kot funkcijo spreminjanja nivoja diskriminacije. Meritev poteka tako, da za vsak nivo diskriminacije preštejemo število zaznanih dogodkov. Primer take meritve je prikazan na sliki 127.



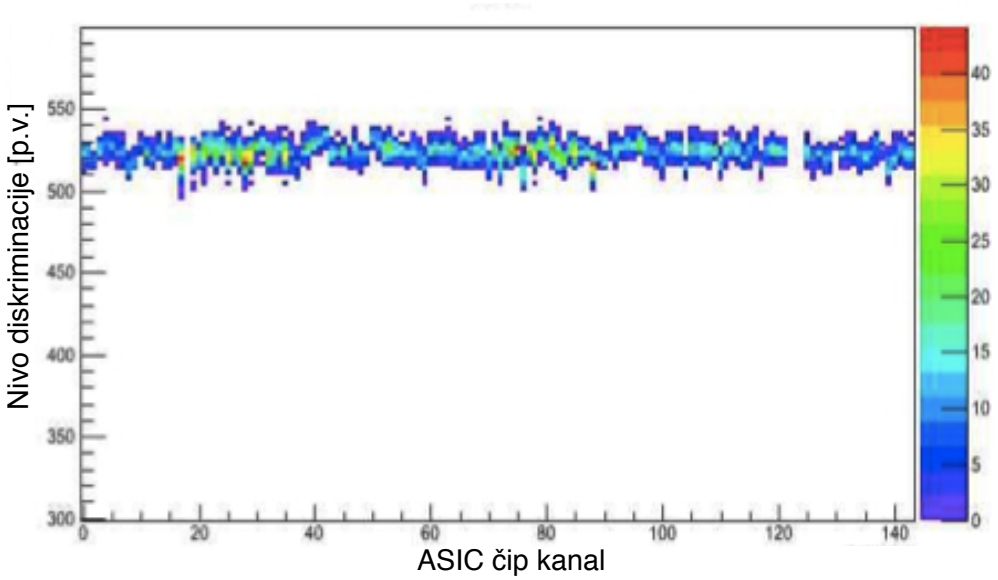
Slika 127: Primer meritve odziva čitalne elektronike kot funkcija spreminjanja nivoja diskriminacije za vseh 144 kanalov z uporabo principa meritve, ki temelji na zaznavanju prehoda.

Preden začnemo z meritvijo je potrebno napravo umeriti. Šumni prispevek vsakega kanala HAPD senzorja je nekoliko različen. Prav tako imajo ASIC čipi nekoliko razmeščene lastne srednje vrednosti. Meritev odziva detektorja kot funkcija spreminjanja nivoja diskriminacije, se uporablja za izračun srednje vrednosti μ in srednjega kvadratnega pogreška σ posameznega kanala. Posamezne kanale želimo poravnati tako, da bo njihov odmik od izbrane vrednosti diskriminacije odmaknjen za 3 do 5 σ razredov.

Kalibracija poteka tako, da najprej v ASIC čipe naložimo privzete vrednosti in izmerimo odziv čitalne elektronike kot funkcijo nivoja diskriminacije. Iz meritve izračunamo potrebne odmike za posamezni kanal. Privzete vrednosti pa prepišemo z novimi vrednostmi.

Sliki 128 in 129 prikazujeta odziv čitalne elektronike kot funkcijo spreminjanja nivoja diskriminacije za princip merjenja štetja prehodov in princip

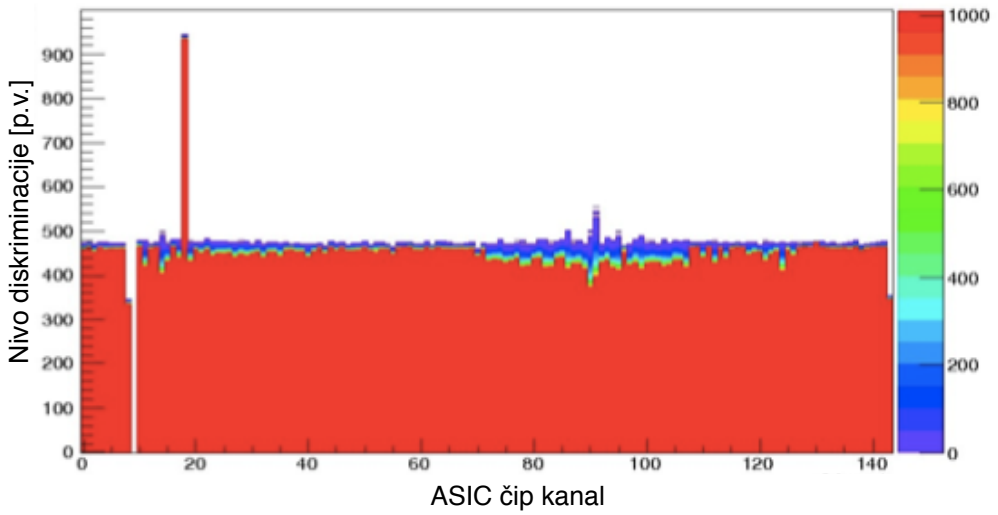
merjenja časa signala nad nivojem diskriminacije.



Slika 128: Umerjena meritev na principu štetja prehodov signala kot funkcija nivoja diskrimnacije. Kanal št 19 prikazuje nepravilno delovanje.

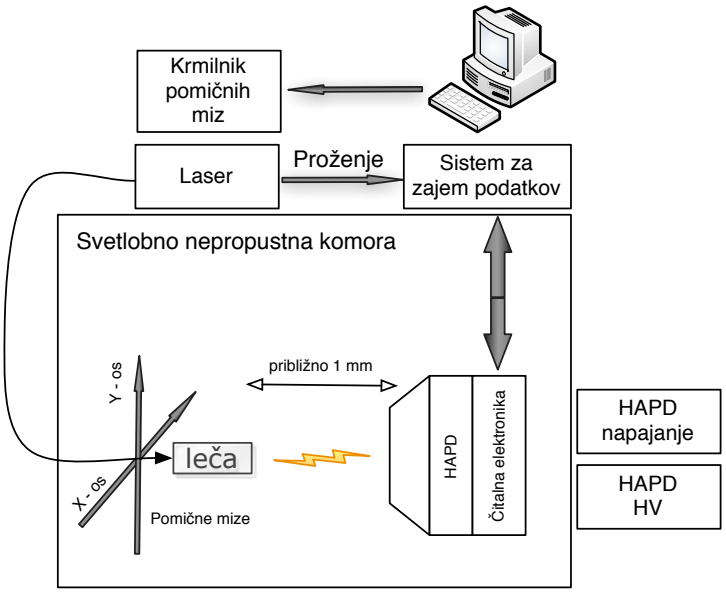
9.3.5 Meritev posameznih fotonov s senzorjem HAPD in primerjava meritev z različnimi principi detekcije

Za preizkus čitalne elektronike z uporabo senzorja HAPD je potreben popolnoma zatemnjen prostor. Uporabili smo zaprto komoro iz aluminija v katero smo namestili senzor HAPD in čitalno elektroniko. Za izvor svetlobe smo uporabili laser valovne dolžine 400 nm. Svetlobo smo v zaprto komoro pripeljali po optičnem vodilu. Točko izvora svetlobe, oddaljeno ≈1 mm od aktivne površine HAPD senzorja, smo premikali s pomočjo računalniško vodenih pomičnih miz. Meritev poteka tako, da laser pri nizki moči sproži svetlobni paket, ki ima v povprečju nekaj fotonov in hkrati sproži sistem za zajem podatkov. Po vsaki meritvi se podatki prenesejo v osebni računalnik. Shematski prikaz preizkusnega mesta je prikazan na sliki 130. Porazdelitev števila fotonov iz svetlobnih izvorov sledi Poissonovi porazdelitvi. Z osvetljevanjem posameznega kanala smo izmerili odziv detektorja kot funkcijo spreminjanja nivoja diskriminacije. Meritev smo opravili za oba principa zajema podatkov. Rezultat je prikazan na sliki 131. Meritev, ki temelji na merjenju časa signala nad nivojem proženja, omogoča rekonstrukcijo osnovnega signala iz oblikovalnika sunkov na ASIC čipu. Sliko lahko rekonstruiramo tako, da merimo število sunkov po celotnem območju vrednosti diskriminacije in izrišemo kot funkcijo zasedenosti bitov v podatkih (Slika 132).

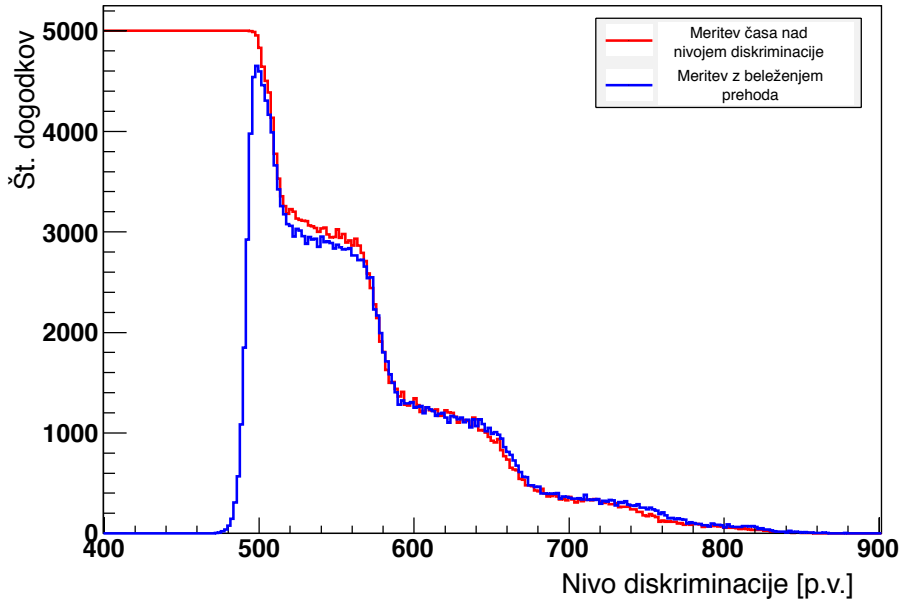


Slika 129: Umerjena meritev na principu merjenja dolžine signala nad pragom kot funkcija nivoja diskriminacije.

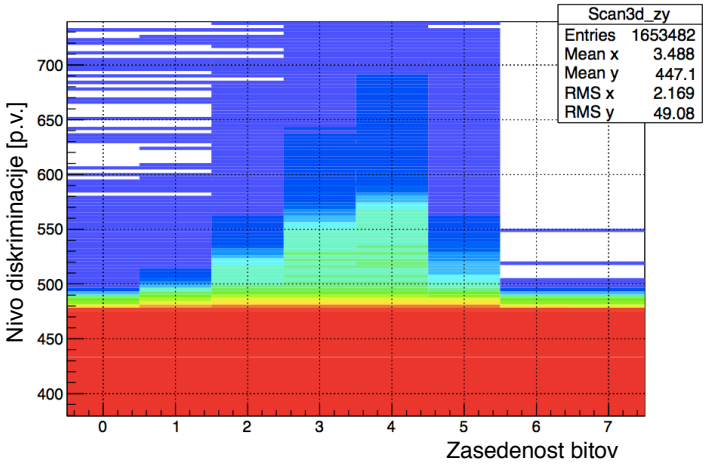
Takšna meritev lahko grobo rekonstruira analogni signal na izhodu iz oblikovalnika sunkov. Cilj uporabe merjenja časa signala nad nivojem proženja omogoča dodatni nivo diskriminacije glede na časovno trajanje signala. Ob ustrezni nastavitvi ure za pomični register je tako mogoče ločevati sunke, ki pripadajo posameznim fotonom in daljše sunke, ki so posledica zadetka fotonov Čerenkova iz kvarčnega stekla senzorja HAPD. Čitalna elektronika vsebuje vezje za generiranje testnih pulzov, ki omogoča kontrolirano vbrizganje naboja na vhod kanala v ASIC čipu. Izmerili smo verjetnost zasedenosti bitov kot funkcijo naboja izraženo v enotah posameznih fotonov. Trajanje posameznega bita je ekvivalentno času 250 ns (Slika 133).



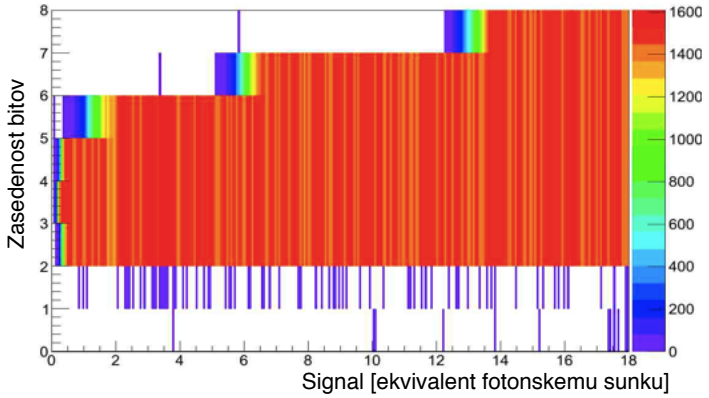
Slika 130: Preizkusno mesto za senzor HAPD in čitalno elektroniko.



Slika 131: Odziva detektorja na posamezne fotone kot funkcija spreminjanja nivoja diskriminacije. Meritev na principu detekcije prehoda in meritev na principu merjenja časa signala nad nivojem diskriminacije.



Slika 132: Verjetnostna porazdelitev zasedenih bitov posameznega kanala kot funkcija nivoja diskriminacije za posamezne fotone.

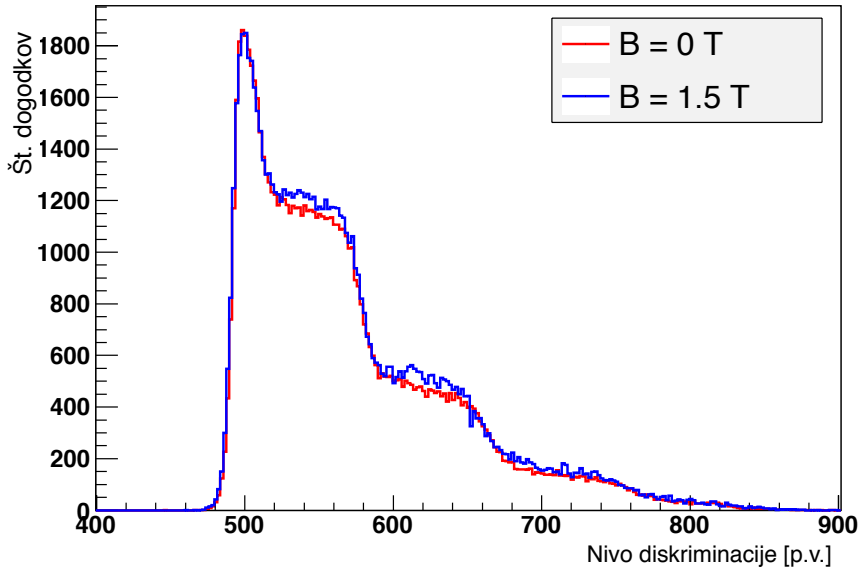


Slika 133: Verjetnost zasedenosti posameznih bitov kot funkcija naboja izražena v enotah fotonskih sunkov - 8 bitov predstavlja okno 2 μs.

9.3.6 Preizkus delovanja v magnetnem polju

V inštitutu KEK v Cukubi na Japonskem smo preizkusili delovanje čitalne elektronike v magnetnem polju 1.5 T, ki ga generira 80 kW elektromagnet. Znotraj jarma je magnetno polje približno homogeno. Senzor HAPD s čitalno elektroniko smo vgradili v svetlobno nepropustno komoro katero se delno vstavi v območje magnetnega polja. Merilno mesto omogoča premikanje izvora fotonov po celotni aktivni površini HAPD senzorja. Primerjava odziva detektorja, kot funkcija spreminjanja nivoja diskriminacije za posamezni kanal brez in v prisotnosti magnetnega polja, je prikazana na sliki 134.

V magnetnem polju ima senzor HAPD nekoliko boljši izkoristek. Foto elektroni pospešeni v električnem polju znotraj senzorja HAPD se vrtinčijo



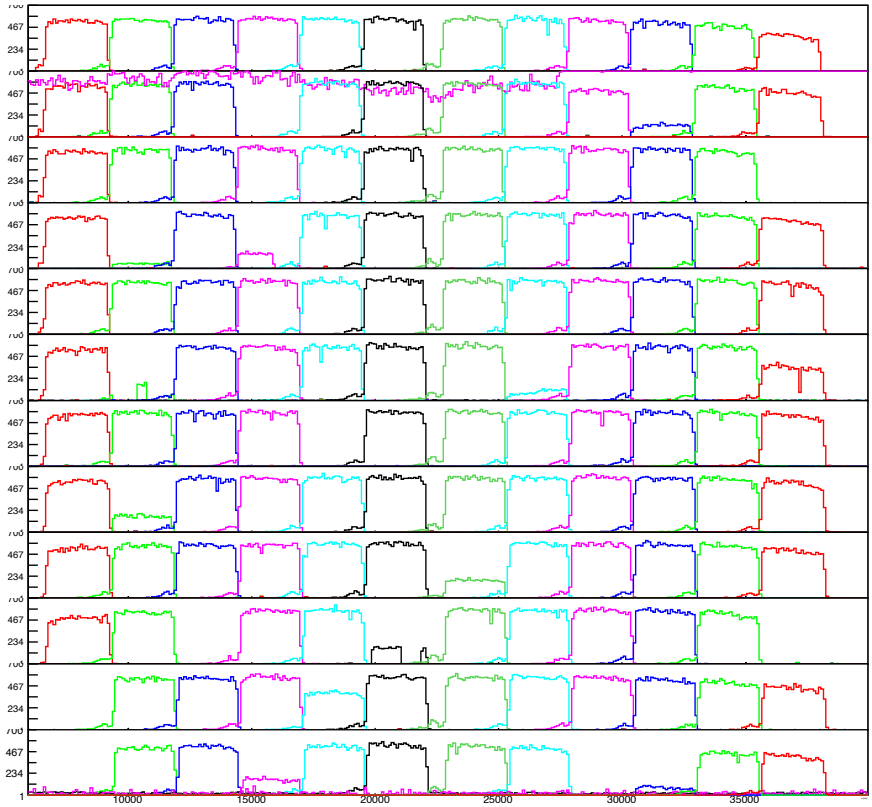
Slika 134: Primerjava odziv detektorja kot funkcija spreminjanja nivoja diskriminacije za posamezni kanal brez in v prisotnosti magnetnega polja na principu zaznavanja prehoda.

okrog silnic magnetnega polja. Kot posledica se v magnetnem polju zmanjša povratno sipanje foto elektronov na sosednje kanale plazovnih foto diod. Magnetno polje pripomore k temu, da se izsipani elektron zbere na istem pikslu. V nasprotnem primeru se fotoelektroni delno sipljejo na sosednje kanale [32]. Preverili smo odziv celotnega senzorja HAPD po aktivni površini z uporabo čitalne elektronike. Izvor svetlobe smo premikali v vrsticah po geometričnih centrih kanalov in merili skupno število zadetkov. Slika 135 prikazuje rezultat meritve.

9.3.7 Preizkus delovanja v območju sevanja

V okolju Belle II eksperimenta pričakujemo $\approx 10^{12}$ nevtronov/cm^2 v desetih letih obratovanja. Na najbolj izpostavljenem mestu v ARICH detektorju lahko fluks 1MeV ekvivalentnih nevtronov doseže 2×10^{11}/cm^2/leto. Spekter nevtronov je prikazan na sliki 136. Skupna radiacijsko doza gamma žarkov je ocenjena na 70 Gy v desetih letih. Senzor HAPD je bil predhodno večkrat preverjen. Po več preizkusih različnih HAPD detektorjev smo izbrali najodpornejšega, ki tudi po obsevanju ekvivalentne doze Belle II eksperimenta ohranja naboljše razmerje signal/šum [33].

Čitalna elektronika je sestavljena iz več elektronskih komponent. ASIC čipi so v osnovi projektirani, da vzdržijo zahteve po odpornosti na radiacije. Večjo neznanko predstavlja vezje FPGA in podporna elektronska vezja. Eno



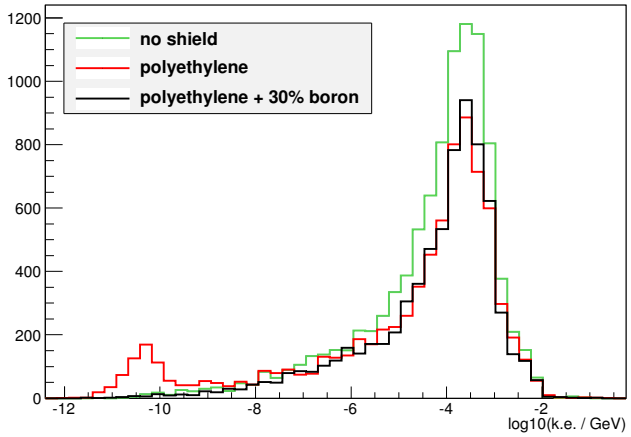
Slika 135: Meritev občutljivosti površine v prisotnosti magnetnega polja 1.5 T. Odziv na fokusirano svetlobo nizke intenzitete (v povprečju posamezni fotoni). Vsaka vrstica na sliki predstavlja meritv po centrih pikslov senzorja HAPD ene vrstice pikslov.

od omejitev za katero nismo vedeli ob izbiri FPGA vezja Spartan 6 predstavlja proizvodnji proces tega čipa. V tem vezju za dopiranje silicijevih rezin uporabljajo element Bor. Termični nevtroni tako predstavljajo težavo pri uporabi tega vezja saj interagirajo z Borom [36].

$$^{10}B + n \rightarrow^{7} Li + \alpha + \gamma(94\%) \quad (31)$$

$$\rightarrow^{7} Li + \alpha(6\%) \quad (32)$$

Čitalna elektronika ni bila pred tem še nikoli preizkušena na odpornost za sevalne poškodbe. Na inštitut Jožef Stefan v Ljubljani smo na reaktorju TRIGA Mark II izvedli več preizkusov obsevanja v različnih časovnih obdobjih. Za preizkus smo uporabili čitalno elektroniko povezano na sistem za zajem podatkov. Preko dveh koaksialnih kablov smo lahko merili analogne signale iz ASIC čipov ter izhodne napetosti iz vezja za diskriminacijo signala. Za programiranje FPGA čipa preko JTAG vodila smo uporabili ločeno povezavo. Zajem podatkov je beležil osebni računalnik.



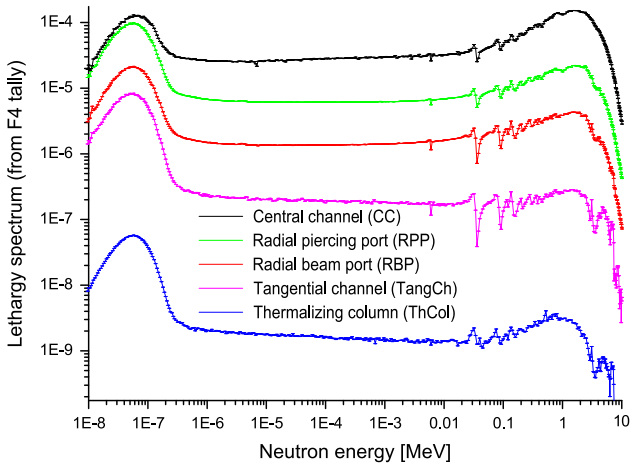
Slika 136: Spekter nevtronov na poziciji ARICH detektorja v spektrometru Belle II [30].

Reaktor ima za obsevanje vzorcev na razpolago več obsevalnih kanalov. Za nas je bila najbolj primerna suha celica. Z merilnimi ELMA diodami smo pri polni moči reaktorja izmerili fluks 3.275×10^6n/s/cm^2 1 MeV ekvivalentnih nevtronov. Radiacijska dozo smo izmerili z 3 termoluminescenčnimi dozimetri pritrjenimi na čitalno elektroniko. Ta znaša 4.3 Gy/uro. Spekter nevtronov v suhi celici je prikazan na sliki 137.

Pri takšnem fluksu nevtronov bi lahko čitalno elektroniko obsevali do končne vrednosti v 85h, kar je približno 700 krat hitreje, kot v eksperimentu Belle II. Najverjetneje predpostavka ne drži popolnoma, saj sta si spektra za nevtrone v Belle II in reaktorju TRIGA različna in učinek termalnih in hitrih (300 keV) nevtronov ni enak. Čitalno elektroniko smo skupno obsevali ekvivalentno štirim Belle II letom brez trajnih poškodb vezja.

Čitalne elektronike pri nizki moči reaktorja izgleda, da deluje brez napak, vendar je lahko to posledica kratkega časa izpostavljenosti. Pri povečani moči reaktorja smo opazovali napake, ki se pojavljajo na vezju. Delovanje vezja za nastavitev nivoja diskriminacije je delovalo pravilno tudi pri povečanem fluks nevtronov pri polni moči reaktorja.

Integrirano vezje FPGA smo preizkusili na več načinov. Program za FPGA, ki ima vgrajen samo sistem za pošiljanje fiksnih podatkov porabi približno 2% logičnih celic vezja. Pri polni moči reaktorja smo ciklično brali podatke. V primeru nepričakovanega rezultata smo ponovno naložili FPGA s programom. Delovanje se za nekaj časa povrne v normalo. Zaznali smo 9.2 napak na uro, kar bi ob uporabi celotnega prostora FPGA zneslo 460 napak na uro. To je približno ekvivalentno 0.65 napake na uro v Belle II okolju. V ARICH detektorju je predvidena uporaba 420 čitalnih vezij. Za dodatno varnost delovanja ARICH detektorja potrebujemo način za preverjanje



Slika 137: Letargijski spekter nevtronov v suhi celici trig reaktorja - ThCol. [35]Letargijski in energijski spekter sta povezana z $\Phi_L = E\Phi_E$.

	SEU klasifikacija	10 kW	100 kW
Popravljiva nebistvena napaka	FC 00	0.05	0.14
Nepopravljiva nebistvena napaka	FC 20	0.1	0.04
Popravljiva bistvena napaka	FC40 -SC10	5.06	3.4
Nepopravljiva bistvena napaka	FC60 -2*SC01	0.15	0.49

Tabela 13: Rezultati štetja sporočil iz SEM krmilnika. Pričakovana stopnja napak v konfiguracijskih bitih čitalne elektronike normiranih na urno postavko v Belle II ARICH okolju.

pravilnosti delovanja FPGA vezja.

Podjetje Xilinx ponuja v programskem okolju možnost integracije ublažitvenega (SEM) krmilnika, ki omogoča odkrivanje in delno odpravljanje napak zaradi induciranih učinkov sevanja. Krmilnik komunicira z zunanjim svetom preko serijskega vodila, ki bazira na komunikaciji po protokolu RS422 in sporoča napake, ki jih je zaznal. Poleg pošiljana sporočil o zaznanih napakah, je v krmilnik mogoče tudi umetno inducirati (z ukazom) napako, za preizkus njegovega delovanja.

Meritev z uporabo SEM krmilnika poteka tako, da najprej naložimo program v FPGA. Vsako minuto umetno vnesemo napako za preizkus delovanja in pregledujemo sporočila pri fiksni moči reaktorja. Sporočila iz krmilnika zapisujemo v datoteko. Ob primeru zaustavitve SEM krmilnika, FPGA ponovno naložimo s programom. Rezultati obsevanja v reaktorju normirani na Belle II fluks nevtronov so zabeleženi v Tabeli 13.

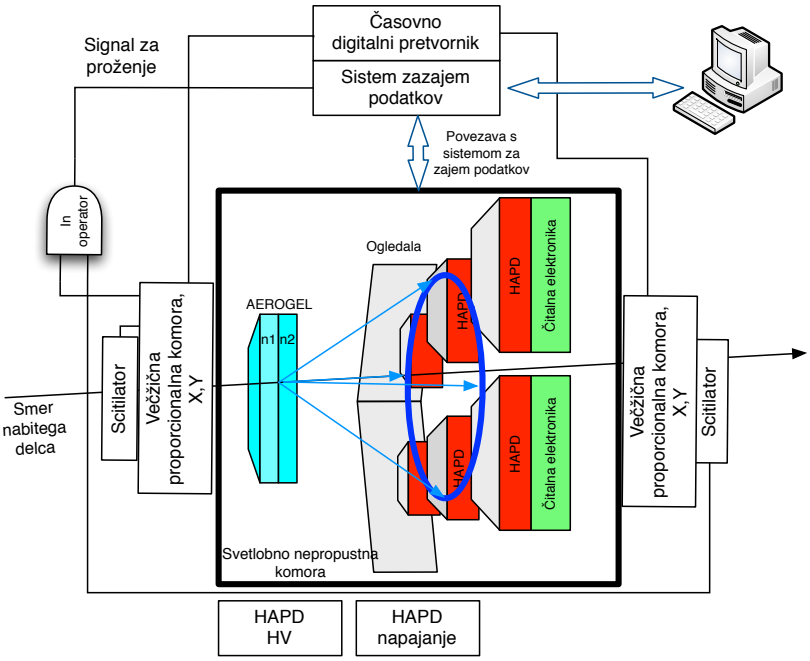
Preizkus FPGA vezja Spartan 6 v suhi celici Triga reaktorja nakazuje možnost njegove uporabe v čitalni elektroniki za ARICH detektor. Do 10 odpovedi delovanja FPGA čipa na uro je še vedno opravičljiv rezultat, saj

nalaganje novega programa traja le nekaj sekund. SEM krmilnik je tako uporaben kot dodatno varovalo delovanja FPGA čipa. Ob sprotnem obveščanju kontrolnega sistema o sevalnih poškodbah omogoča pravočasno preventivno ponovno nalaganje programa in s tem skrajša mrtvi čas delovanja celotnega detektorja.

9.3.8 Preizkus delovanja naprave v curku nabitih delcev

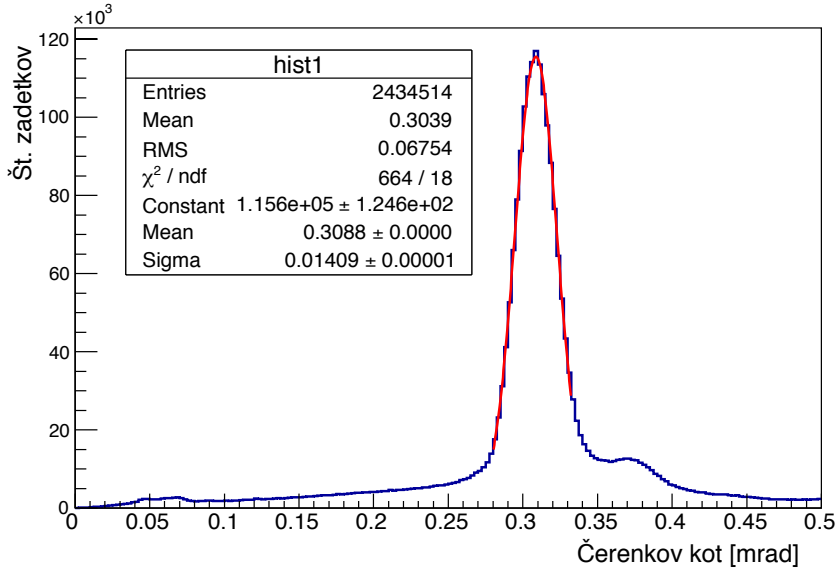
Preizkus detektorja obročev Čerenkova s sevalcem iz aerogela je potekal na evropski organizaciji za nuklearne raziskave CERN v Ženevi, Švica. Na pospeševalniku SPS je na razpolago žarek pionski gibalne količune 120 Gev/c za eksperimente v žarkovnih linija.

Pripravili smo pomanjšano različico ARICH detektorja za preizkus meritve kota Čerenkova. Detektor smo sestavili iz 6 HAPD senzorjev in čitalnie elektronike v zaprti komori z razdaljo 20 cm med sevalcem iz aerogela in detektorsko ravnino. Za merjenje vstopne in izstopne točke nabitih delcev smo uporabili večžične proporcionalne komore. Za proženje dogodkov sta bila uporabljena dva scintilacijska detektorja, ki koincidenčno prožita signal za zajem. Postavitev merilnega mesta je prikazana na sliki 138.



Slika 138: Shematski prikaz postavitve merilnega mesta.

Izmerjeni rezultati so primerljivi z rezultati iz prejšnjih preizkusov v curku nabitih delcev. Izmerjeni Čerenkov kot je prikazan na sliki 139.



Slika 139: Čerenkov kot izmerjen na preizkusu v curku pinov 120 GeV/c.

9.4 Zaključek

Detektor obročev Čerenkova s sevalcem iz aerogela za spektrometer Belle II predvideva uporabo senzorja HAPD za merjenje posameznih fotonov. V doktorski disertaciji sem obravnaval razvoj čitalne elektronike za tak senzor. Čitalna elektronika bo vgrajena v spektrometer Belle II v smeri gibanja masnega težišča razpada produktov trka elektronov in pozitronov pri resonanci $\Upsilon 4(S)$.

Detektor obročev Čerenkova uporablja sevalec iz aerogela z lomnim količnikom $\approx$ 1.05. Pri izbranem lomnem količniku detektor omogoča učinkovito ločevanje pionov in kaonov v območju gibalnih količin od 1 GeV do 4 GeV. Za posamezen nabiti delec z zadostno hitrostjo, ki preleti plast aerogela, pričakujemo približno 10 detektiranih fotonov na aktivni površini detektorja. Za učinkovito merjenje posameznih fotonov s senzorjem HAPD potrebujemo čitalno vezje, ki deluje v magnetnem polju in je med delovanjem odporno na sevanje in nevtrone.

Čitalno elektronsko vezje je sestavljeno iz integriranih vezji za specifične namene, digitalnega vezja FPGA ter podpornih sistemov, ki omočajo nastavitve delovanja. Vezje za specifične namene je sestavljeno iz verige ojačevalnikov in diskriminatorja, ki signal iz posameznega kanala senzorja HAPD pretvorijo v digitalni podatek. Ta se prenese v vezje FPGA in lokalno zabeleži podatke preden ti prenesjo v sistem za zajem podatkov. Digitalno vezje FPGA ima vgrajena dva principa zajema signala iz HAPD senzorja. To sta princip meritve beleženja dogodka in meritev signala nad

nivojem diskriminacije za posamezni dogodek. Za oba principa zajema smo dobili primerljive rezultate. Podporna vezja na čitalni elektroniki omogočajo učinkovito preverjanje delovanja celotne elektronike iz nadzornega sistema brez potrebe fizičnega dostopa v spektrometer.

Delovanje Čitalnega vezje smo preizkusili v prisotnosti magnetnega polja in izpostavili v fluks nevtronov. Končni preizkus smo naredili z manjšo različico detektorja, ki vsebuje 6 senzorjev HAPD, v fluksu nabitih delcev. Preizkusi čitalne elektronike v laboratoriju so potrdili pravilno delovanje celotnega elektronskega sistema. Odziv senzorja HAPD in čitalne elektronike smo preverili s pomočjo elektromagneta, ki ustvari magnetno polje 1.5 T. Rezultati so v skladu s pričakovanji. Rezultati obsevanja čitalne elektronike z nevtroni in gamma sevanjem omogočajo uporabo takšnega sistema v pogojih delovanja spektrometra Belle II ob pogoju, da se neprestano vrši pregledovanje FPGA vezja pred sevalnimi poškodbami. Pričakujemo, da bo v detektorju ARICH potrebno program za vsako od 420 čitalnih elektronik obnoviti nekajkrat na uro. Dosedanji preizkusi z obsevanjem kažejo, da pri predvideni stopnja sevanja v spektrometru Belle II ta ne bo permanentno poškodovala intgeriranih vezij.

Pri preizkusu detektorja obročev Čerenkova s sevalcem iz aerogela v curku nabitih delcev smo izmerili primerljive rezultate s prejšnjimi preizkusi, ki potrjujejo sposobnost detektorja, da ločuje pione od kaonov pri 4 GeV z natančnostjo 4σ.

Detektor obročev Čerenkova bo vgrajen v spektrometer Belle II leta 2016 pri pospeševalniku SuperKEKB v Cukubi na Japonskem.

10 Bibliography

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Appendices

A Abbreviations

Still to be defined an alphabetic order.

Verilog -standardized as IEEE 1364 a hardware description language (HDL)
VHDL -hardware description language (HDL)
DSP - digital signal processor
CPU - central processing unit
BGA - Ball grid array
LTCC - low temperature coffered ceramic
MSB - most significant bit
LSB - less significant bit
SPI - serial peripheral interface
ARICH - Aerogel Rich Imageing Cherenkov detector
ASIC - Application Specific Integrated Circuit
ACC -Aerogel Cherenkov counter
APD -Avalanche photo diode
CSA - Charge sensitive amplifier
CDC - Central drift chamber
DAQ -Data acquisition
FPGA - Field programmable gate array
Firmware - Referes to executable code for micro processors or FPGA devices
FIT - Failure in time
HAPD - Hybrid Avalanche Photo Diode
FIT - Failure in time
PID - Particle identification device
SA02 -Referes to the ASIC version 2 chip used on readout electronics board
SA03 -Referes to the ASIC version 3 chip used on readout electronics board
SA02 board -Referes to the readout electronics with SA02 chips
SA03 board -Referes to the readout electronics with SA03 chips
SEU - Single event upset
Shaper - CR - RC analog signal filter
SPI - Serial peripheral bus
Software - Referes to executable code for personal computers (Windows,Linux)
TOT - Time over threshold

B S02 board construction

The SA02 board is made out of 12 layers.

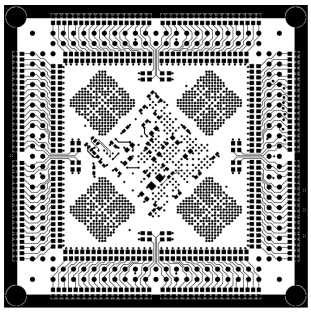

Figure 140: Top layer

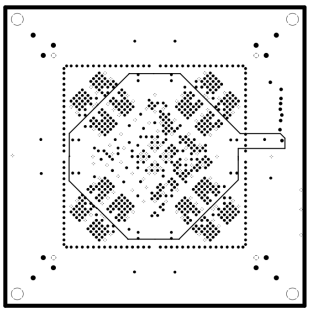

Figure 141: Gnd1

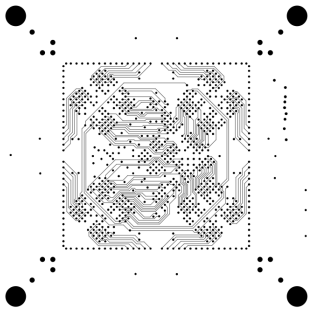

Figure 142: Analog signal1

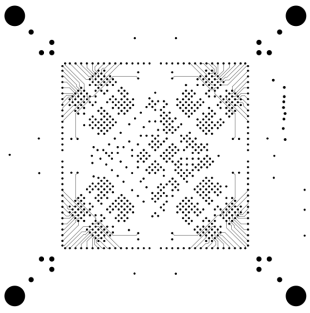

Figure 143: Analog signal2

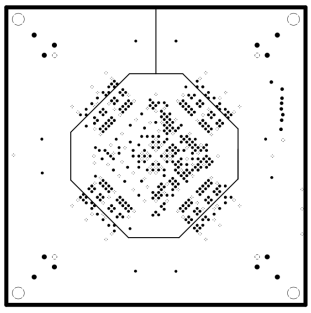

Figure 144: Gnd2

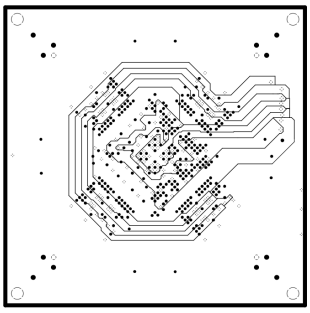

Figure 145: Power plane

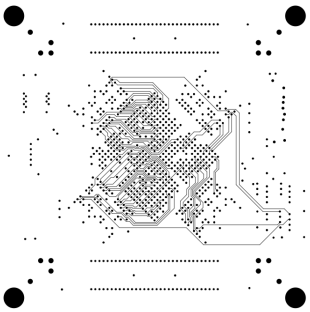

Figure 146: Signal3

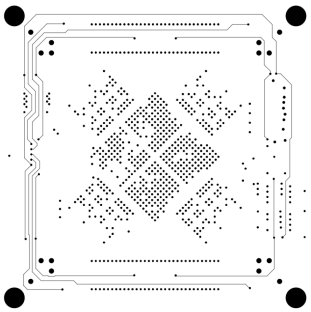

Figure 147: Signal4

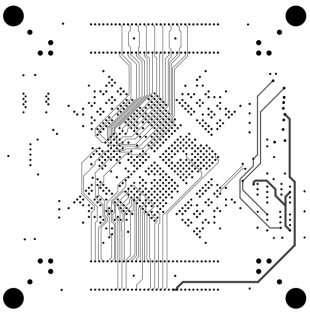

Figure 148: Signal5

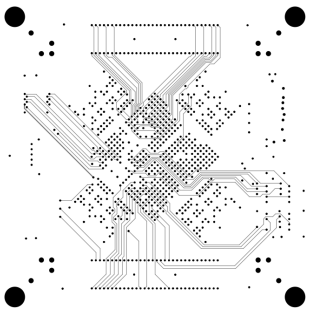

Figure 149: Signal6

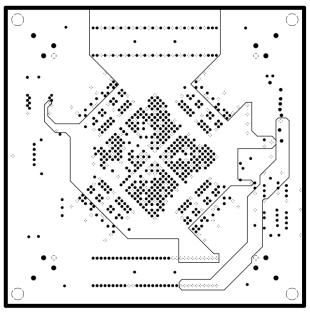

Figure 150: Gnd3

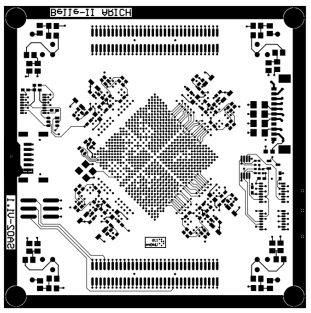

Figure 151: Bottom plane

C Firmware instruction list

* †

*SA03 is a successor of SA02 chip. SA03 ASIC is pin compatible but has a different shaping time setting and a different parameter read back mechanism.

†default value

Name	ID Address	Data bit setting	Range
Slow control			
DAC1A (VTH0)	x05	41- 32	(0x0 to 3FF)
DAC1B (VTH1 - ASIC threshold)	x06	41- 32	(any, range 3FF)
DAC2A (TP)	x07	41- 32	0x0 †
DAC2B (TP1)	x08	41- 32	0x64 †
Asic setup			
Asic1 global param, write	x09	47- 22	(see Asic details)
Asic1 global param, read	x89	47- 22	(SA03 only *)
Asic1 channel param, write	x0A	39- 22	(see Asic details)
Asic1 channel param, read	x8A	39- 22	(SA03 only *)
Asic1 select monitor channel	x0B	46- 41	(see Asic details)
Asic2 global param, write	x0C	47- 22	(see Asic details)
Asic2 global param, read	x8C	47- 22	(SA03 only *)
Asic2 channel param, write	x0D	39- 22	(see Asic details)
Asic2 channel param, read	x8D	39- 22	(SA03 only *)
Asic2 select monitor channel	x0E	46- 41	(see Asic details)
Asic3 global param, write	x0F	47- 22	(see Asic details)
Asic3 global param, read	x8F	47- 22	(SA03 only *)
Asic3 channel param, write	x10	39- 22	(see Asic details)
Asic3 channel param, read	x90	39- 22	(SA03 only *)
Asic3 select monitor channel	x11	46- 41	(see Asic details)
Asic4 global param, write	x0F	47- 22	(see Asic details)
Asic4 global param, read	x8F	47- 22	(SA03 only *)
Asic4 channel param, write	x10	39- 22	(see Asic details)
Asic4 channel param, read	x90	39- 22	(SA03 only *)
Asic4 select monitor channel	x11	46- 41	(see Asic details)
Diagnostic			
Mux	0x04	41- 40	(range 3)
TMP1, read only	0x15	not relevant	(any)
TMP2, read only	0x16	not relevant	(any)
Readout			
Test Pulse	0x02	40	0 or 1
Position readout	0x03	44- 40	0 to 5
Shift clock	0x17	42- 40	0 to 5
Send clock	0x18	42- 40	0 to 5
Monitor digital channel	0x19	47- 40	0 to 143
Readout mode	0x1A	41-40	0,1 or 3

Table 14: System instruction list

D SA02 - DAQ wiring diagram

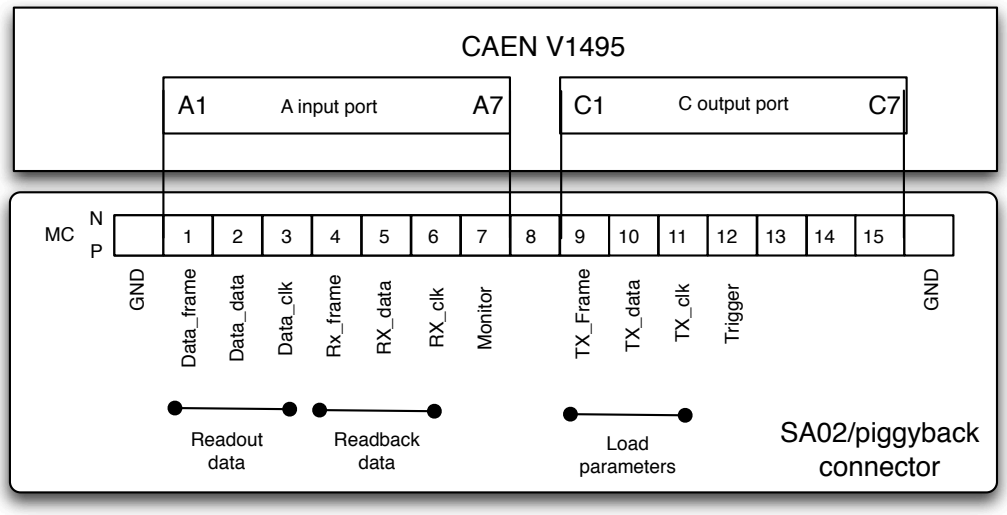

Figure 152: SA02 - DAQ wiring diagram

Izjavljam, da je disertacija rezultat samostojnega raziskovalnega dela.

Ljubljana, december 2013

Andrej Seljak